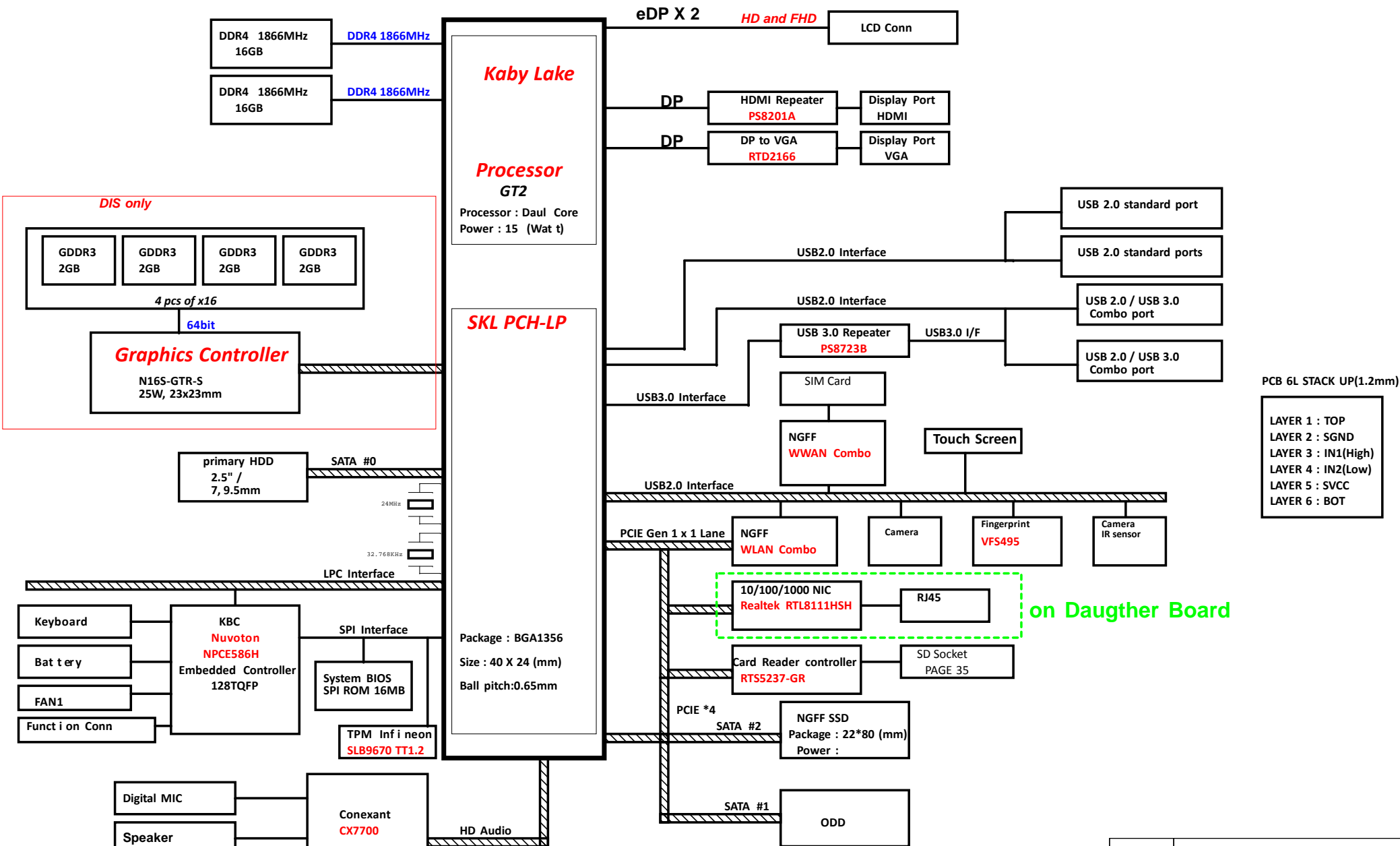
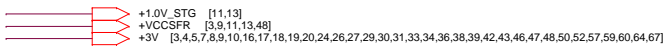
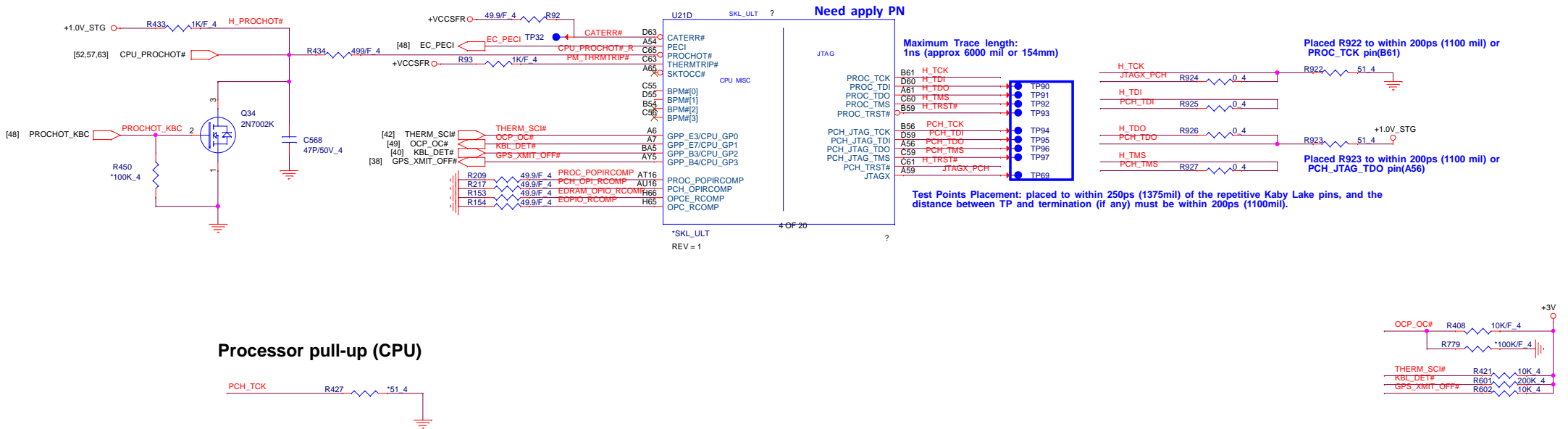
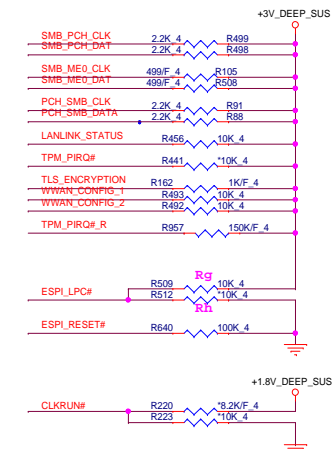


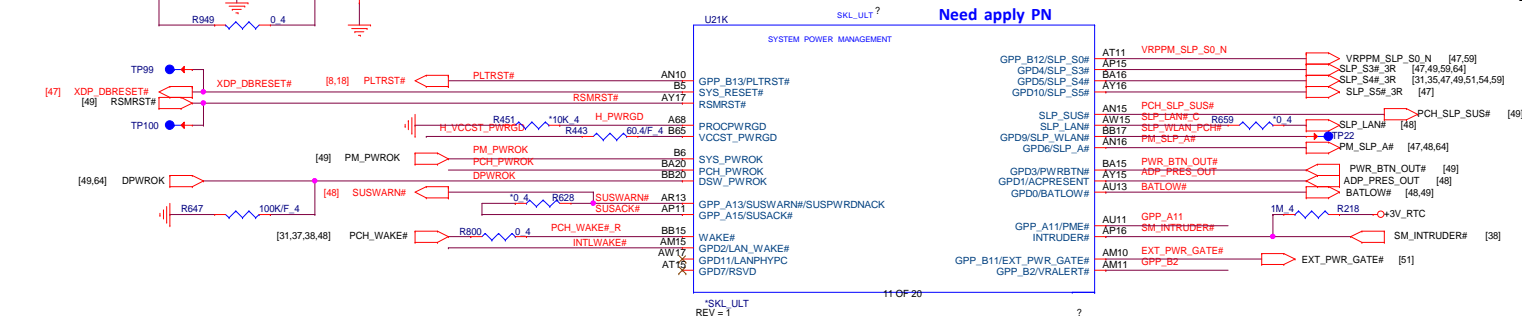
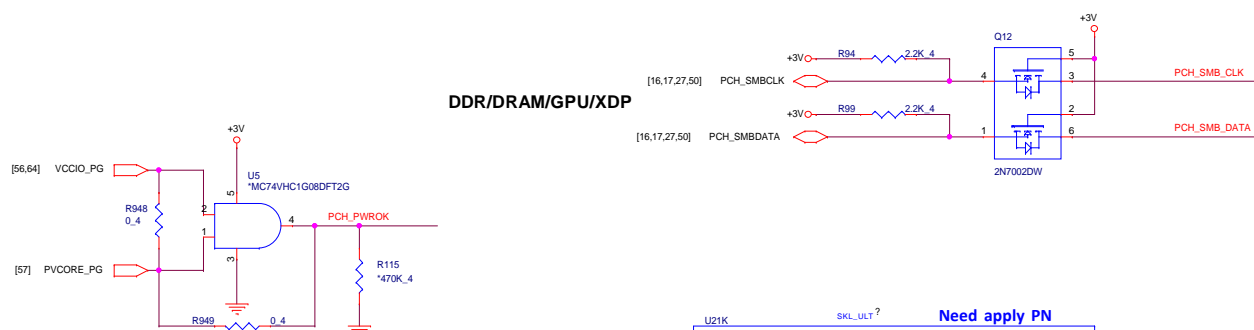
# 2015 400 series Kaby Lake 15"/ 17" (UMA/DIS) Block Diagram 01



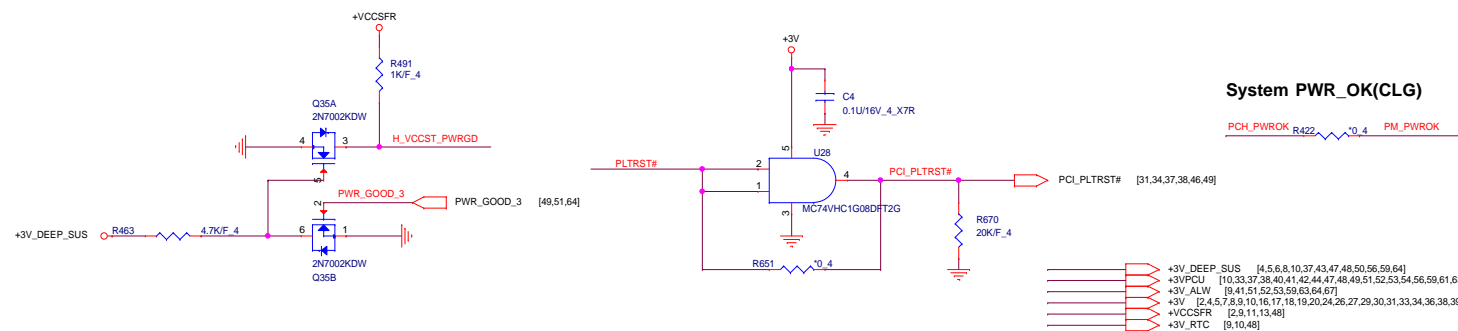
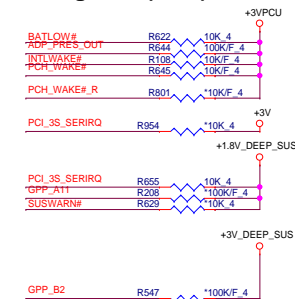




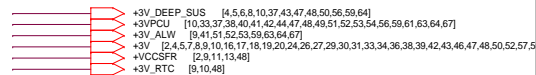
LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R660	<b>Ra</b> 0Ω	15Ω
R662	<b>Rb</b> 0Ω	15Ω
R661	<b>Rc</b> 0Ω	15Ω
R646	<b>Rd</b> 0Ω	15Ω
R653	<b>Rf</b> UNINSTAL	INSTAL
R509	<b>Rg</b> UNINSTAL	INSTAL
R512	<b>Rh</b> INSTAL	UNINSTAL



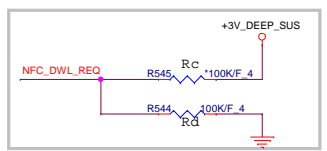
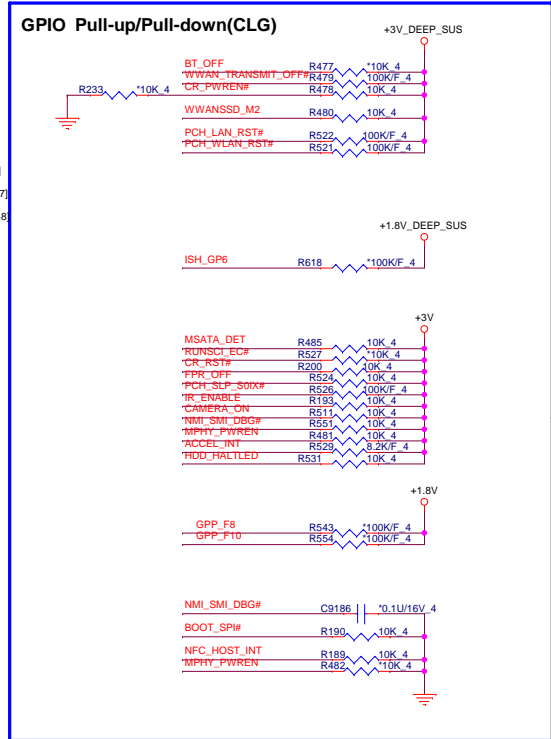
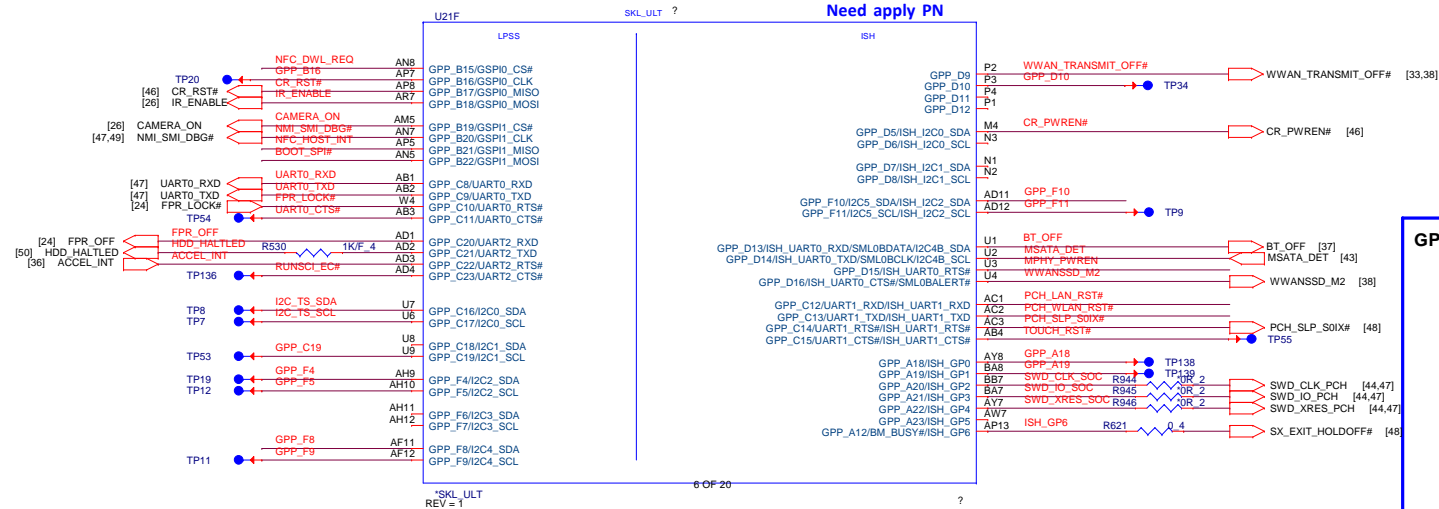
### PCH Pull-high/low(CLG)



**System PWR\_OK(CLG)**




Skylake (GPIO)



Conexant CX7501 & CX7700 TABLE (SI stage)		
	CX7501	CX7700
Rc	UNINSTALL	INSTALL
Rd	INSTALL	UNINSTALL

- +1.8V [5,8,30,55,64]
- +3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
- +3V\_DEEP\_SUS [3,5,6,8,10,37,43,47,48,50,56,59,64]
- +3V [2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

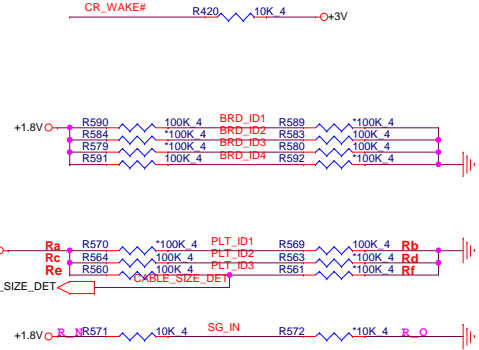
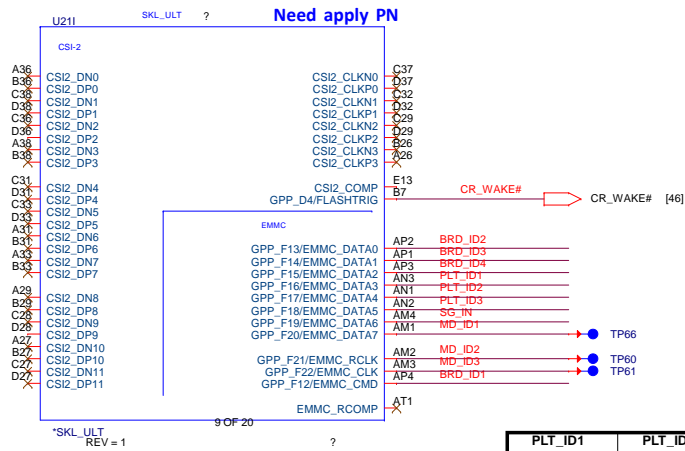


**PROJECT : X63**

**Quanta Computer Inc.**

Size Custom	Document Number 04 – SKYLAKE (GPIO)	Rev 1A
Date: Thursday, May 19, 2016	Sheet 4 of 67	

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	1	1	1	
SI	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



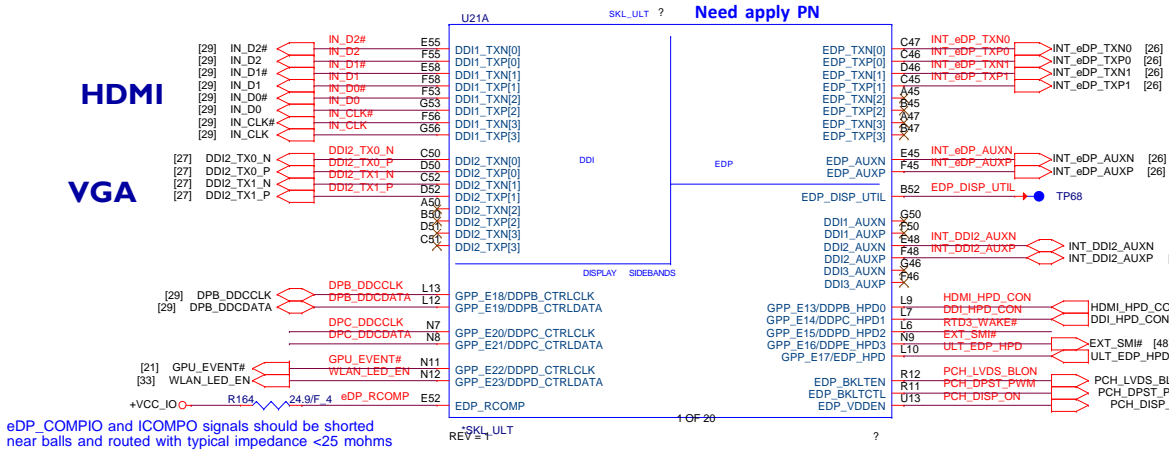
PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	1	15.6"
0	1	1	17.3"

SG_IN	Install	Un-Install
UMA	R572 R_O	R571 R_N
DIS	R571 R_N	R572 R_O

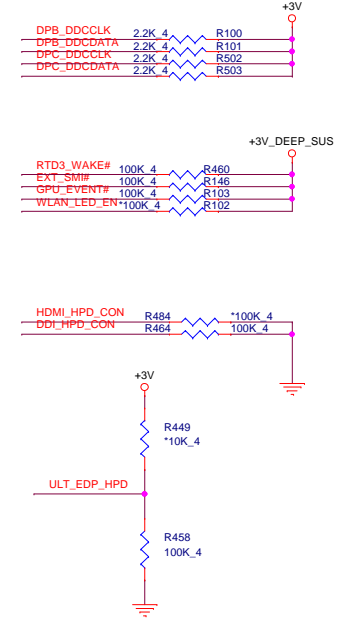
Cable detect

HDMI

VGA

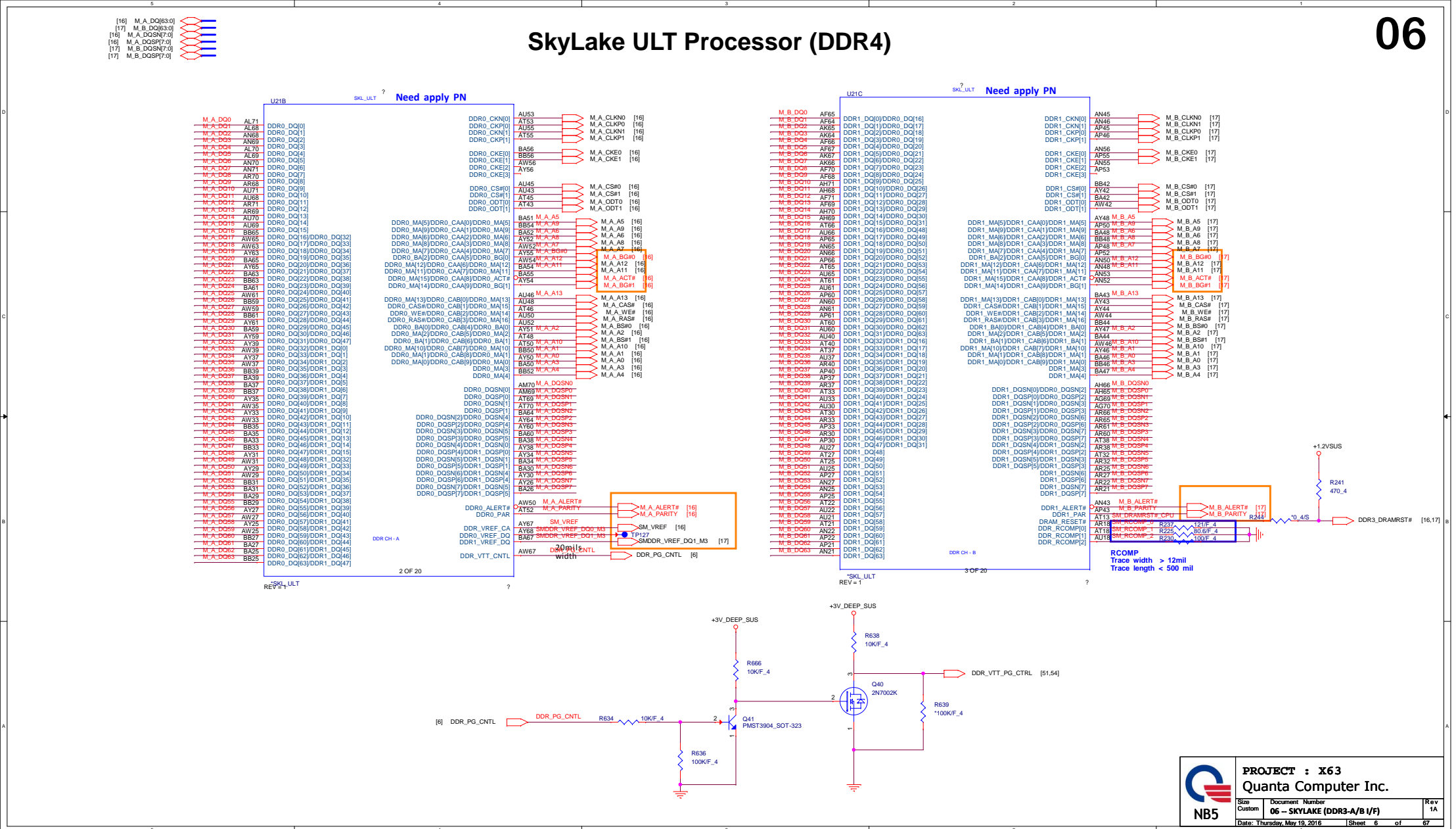


eDP

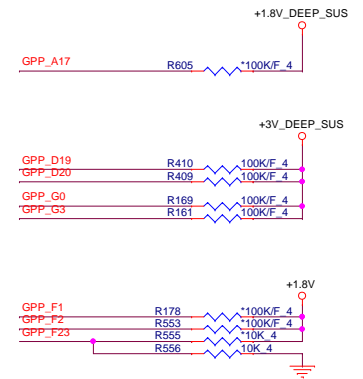
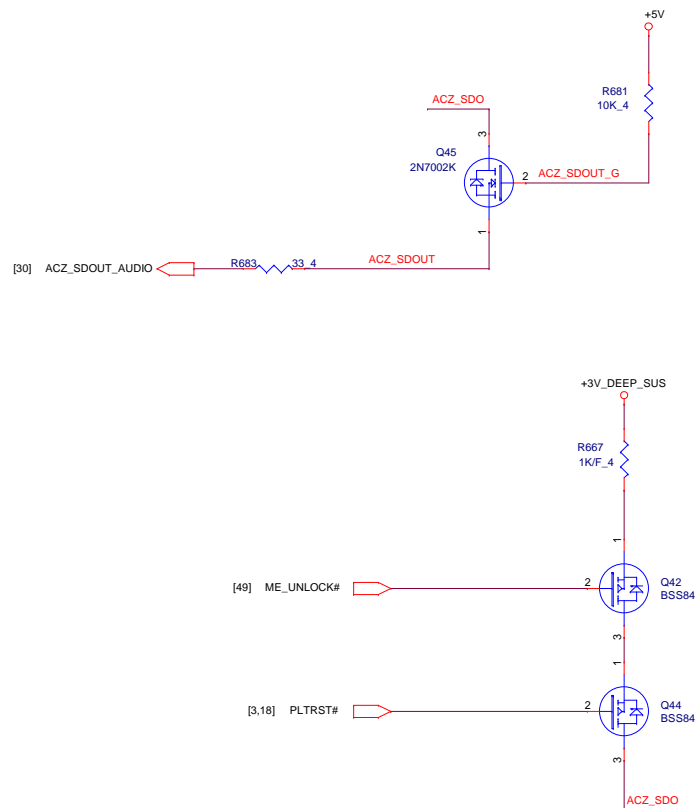
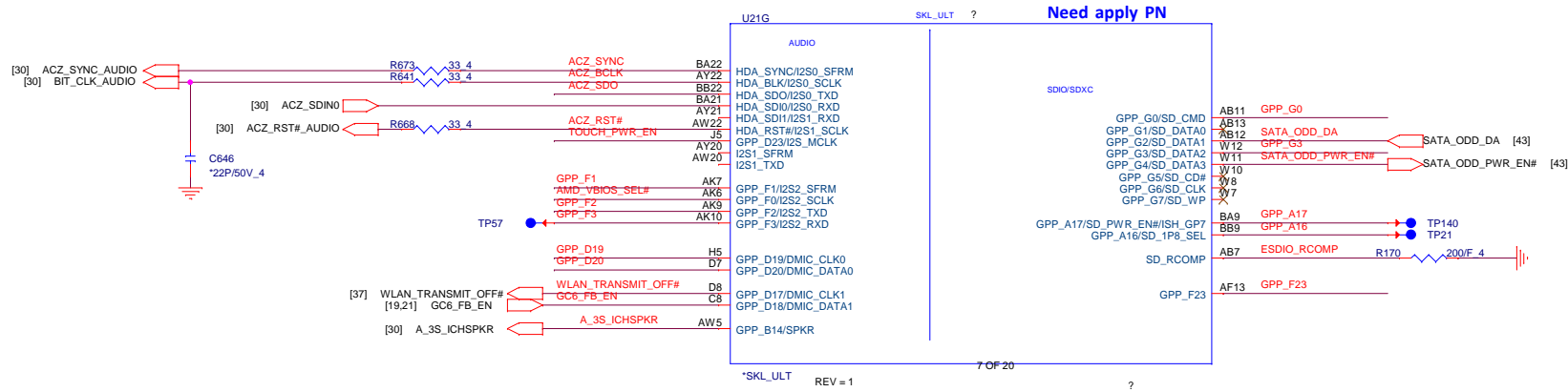


eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

## SkyLake ULT Processor (DDR4)



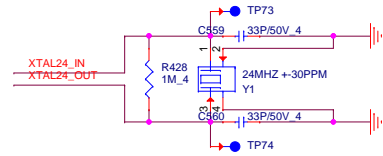
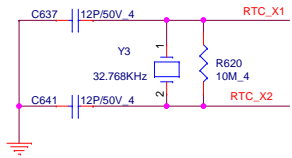




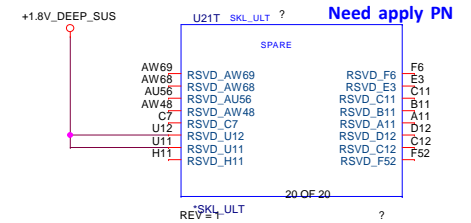
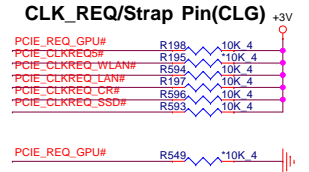
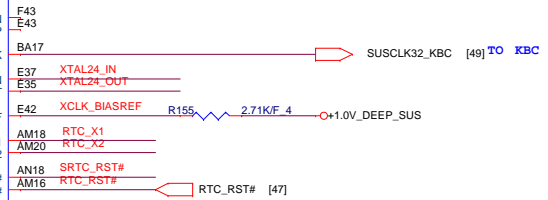
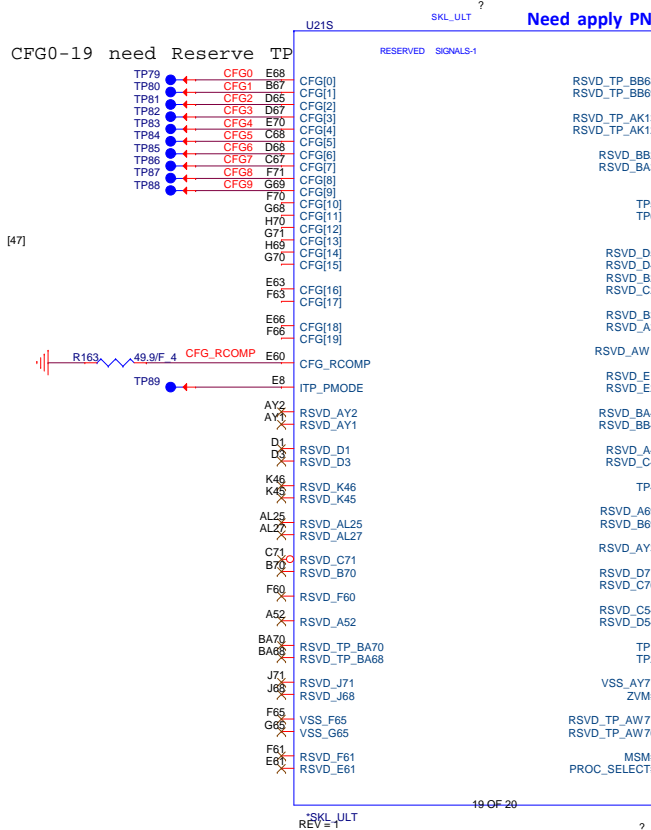
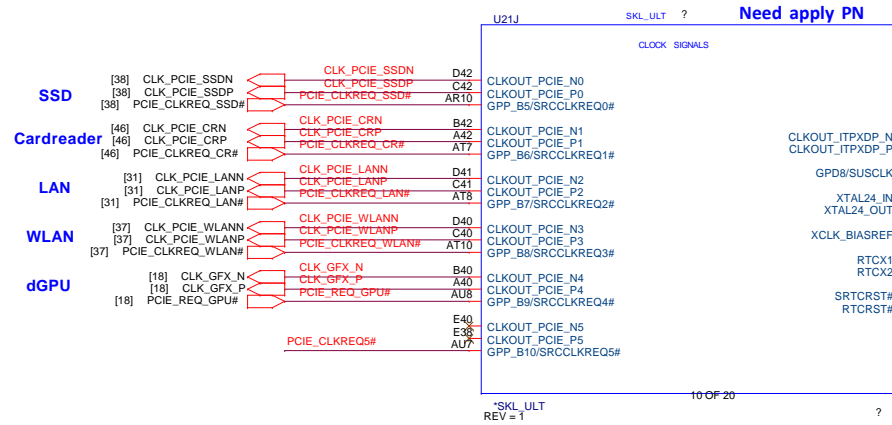
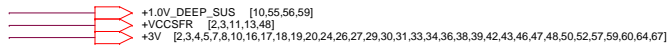
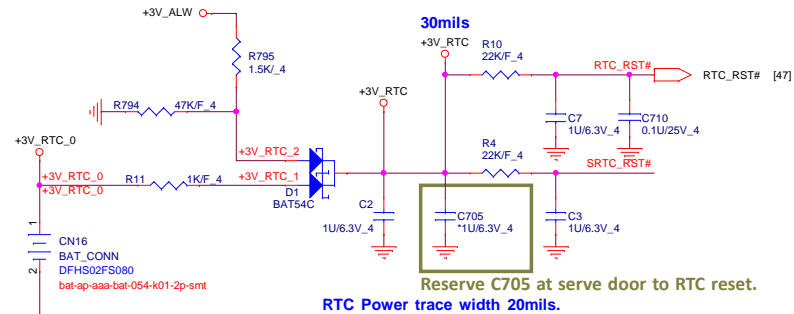
AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	



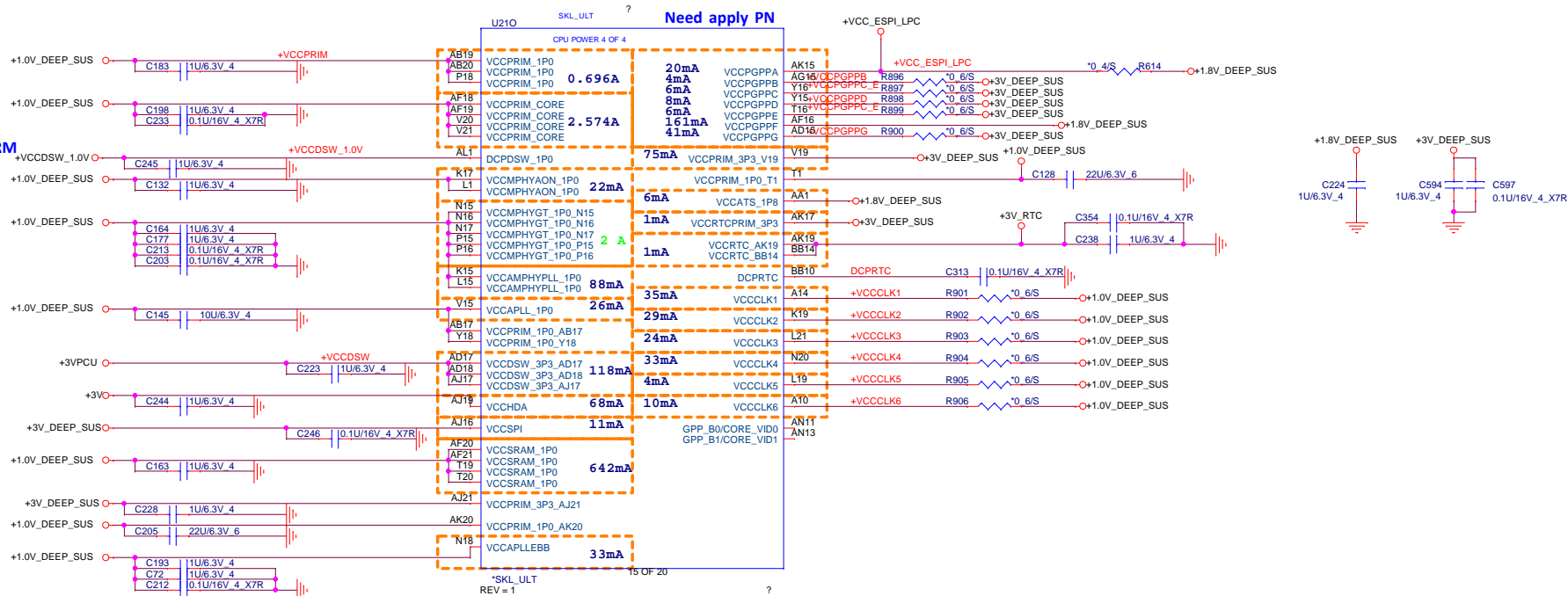
### RTC Clock 32.768KHz



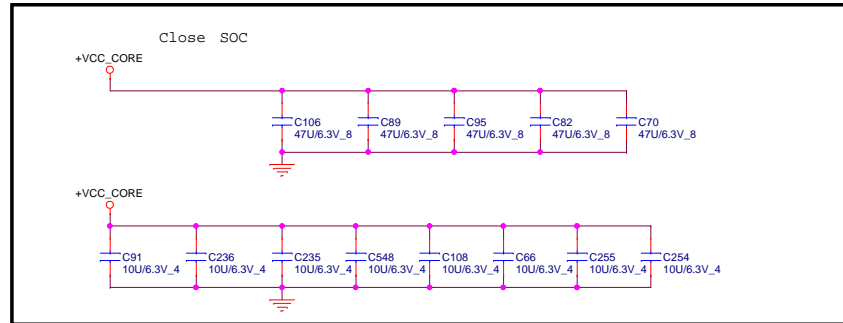
### RTC Circuitry(RTC)



## PCH Internal VRM



+3V\_DEEP\_SUS [3,4,5,6,8,37,43,47,48,50,56,59,64]  
+3VPCU [3,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]  
+1.0V\_DEEP\_SUS [9,55,56,59]  
+VCC\_PRIM  
+3V [2,3,4,5,7,8,9,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]  
+1.8V\_DEEP\_SUS [3,4,7,8,9,48,50,55,64]



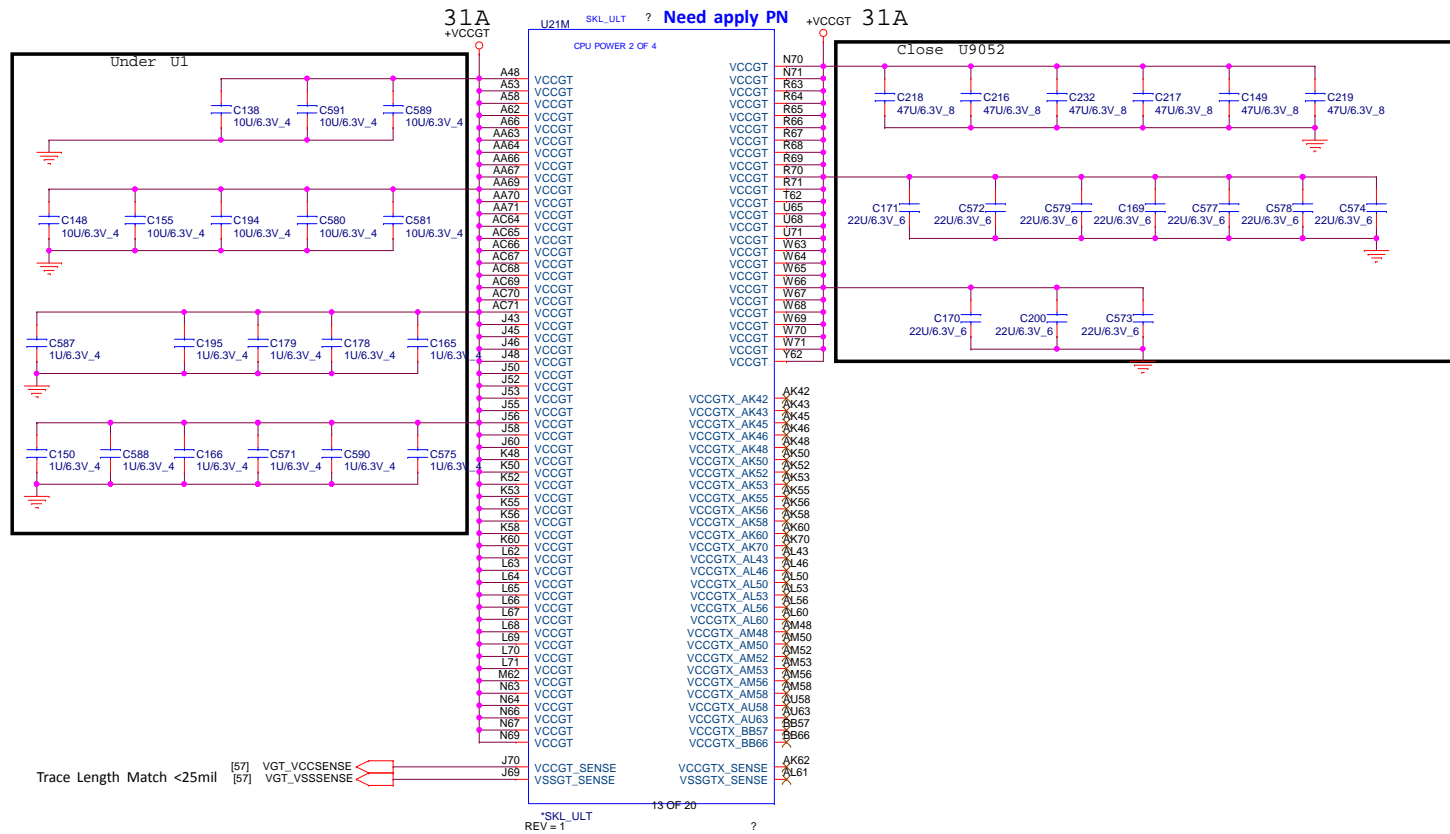
The diagrams illustrate the correct placement of pull-up resistors for SVID signals in a system with a CPU and a VR module. Each diagram shows a signal line connected to a pull-up resistor (R82, R85, R89) which is then connected to a +VCCSFR supply. The signal lines are labeled with their respective names and bus widths.

**Diagram 1: SVID ALERT**  
 - **Layout note:** need routing together and ALERT need between CLK and DATA.  
 - **Annotations:** "CLOSE TO CPU PLACE THE PU RESISTORS" (near R82), "SVID ALERT" (in red).  
 - **Components:** Resistor R82 (56.2/F<sub>4</sub>), capacitor C85 (0.1U/16V<sub>4</sub> X7R).  
 - **Signal:** H\_CPU\_SVIDALRT# [57] connected to VR\_SVID\_ALERT# [57].

**Diagram 2: SVID CLK**  
 - **Annotations:** "PLACE THE PU RESISTORS CLOSE TO VR PULL UP IS IN THE VR MODULE" (in blue), "SVID CLK" (in red).  
 - **Components:** Resistor R85 (54.9/F<sub>4</sub>).  
 - **Signal:** VR\_SVID\_CLK connected to VR\_SVID\_CLK [57].

**Diagram 3: SVID DATA**  
 - **Annotations:** "CLOSE TO CPU PLACE THE PU RESISTORS" (in blue), "SVID DATA" (in red).  
 - **Components:** Resistor R89 (100/F<sub>4</sub>).  
 - **Signal:** VR\_SVID\_DATA connected to VR\_SVID\_DATA [57].







Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCI<sub>O</sub></sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

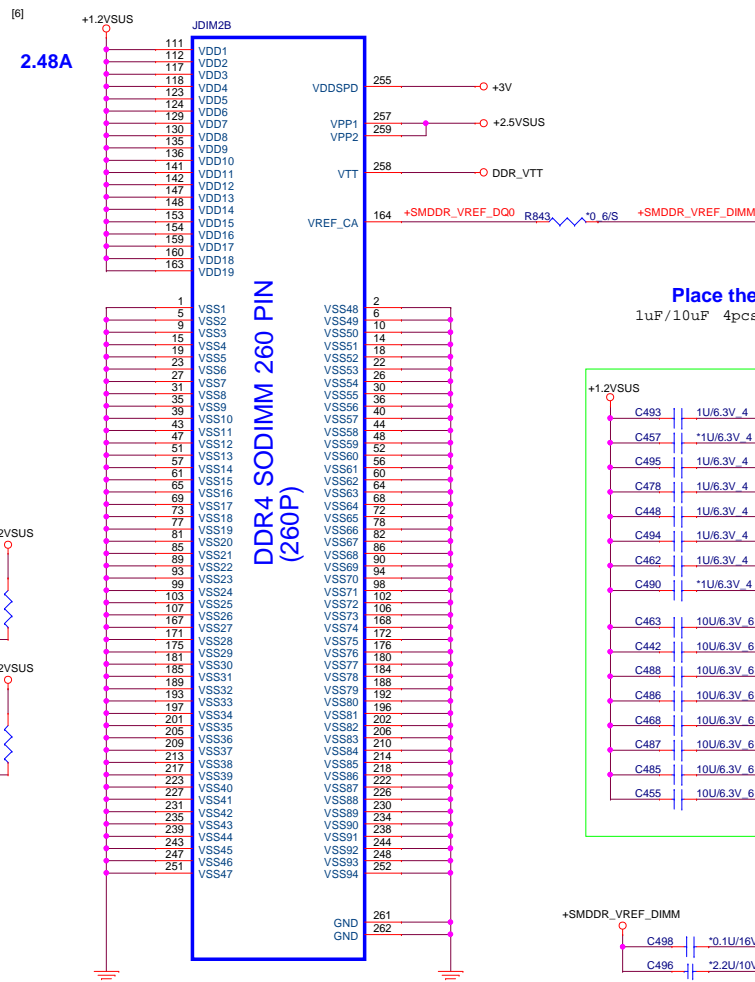
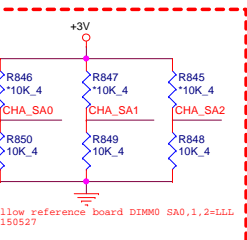


10/28 Del XDP

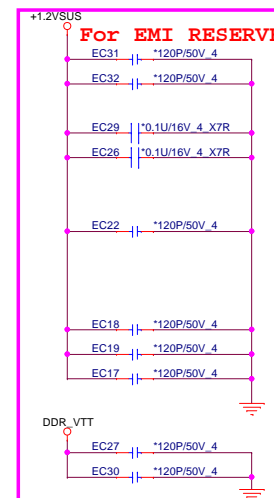
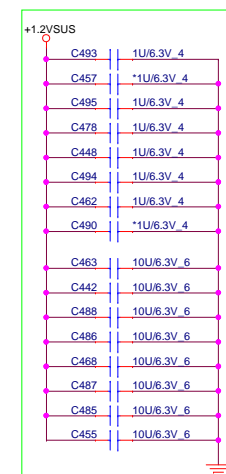
11/03 Del XDP

PV, 0421 Delete APS Connector

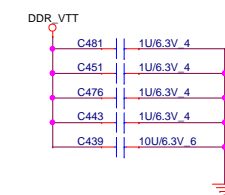
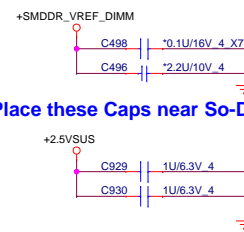
11/03 Del XDP



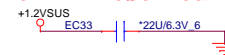
**Place these Caps near So-Dimm0.**  
1uF/10uF 4pcs on each side of connector



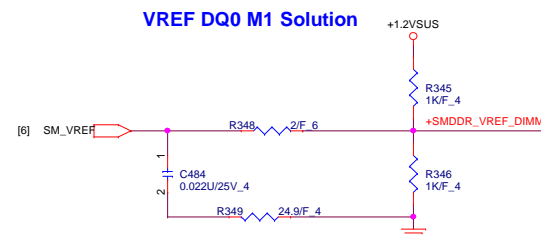
**Place these Caps near So-Dimm0.**



For RF Reserved



### VREF DQ0 M1 Solution



[2,3,4,5,7,8,9,10,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

[6,13,17,54,59,61] +1.2VSUS  
[17,54,59] DDR\_VTT

+3V  
2VSUS  
TT





[illegible]

The schematic diagram illustrates the PLL power supply network. A +3V<sub>AON</sub> input is connected to a network of capacitors (C1052, C1053, C1054) and inductors (L1052, L1053, L1054) located near the GPU. The network is connected to the PLL power pins: AA8, AA9, and AB8. AA8 and AA9 are connected to PEX\_PLL\_HVDD, and AB8 is connected to PEX\_SVDD\_3V3.

The diagram shows two digital signals over time. The top signal is labeled `[60] GPU_VCC_SENSE` and has a red arrow pointing left, indicating a falling edge. It is connected to a line labeled `F2`, which then connects to `VDD_SENSE`. The bottom signal is labeled `[60] GPU_VSS_SENSE` and has a red arrow pointing right, indicating a rising edge. It is connected to a line labeled `F1`, which then connects to `GND_SENSE`. Both signals are shown as high-frequency digital pulses.

Diagram illustrating the PEX PLLVDD and TESTMODE connections for the CX300T30001.

**PEX\_TSTCLK and PEX\_TSTCLK#:** Connected to AF22 and AE22. Note: \*200F/4 R1007. CX300T30001 Change to 0ohm.

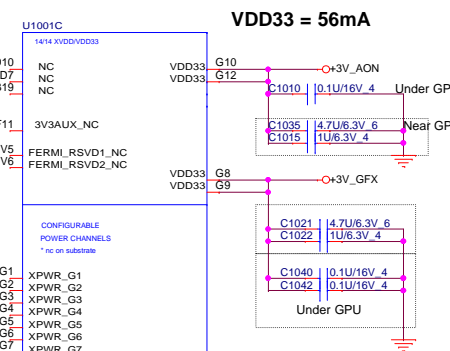
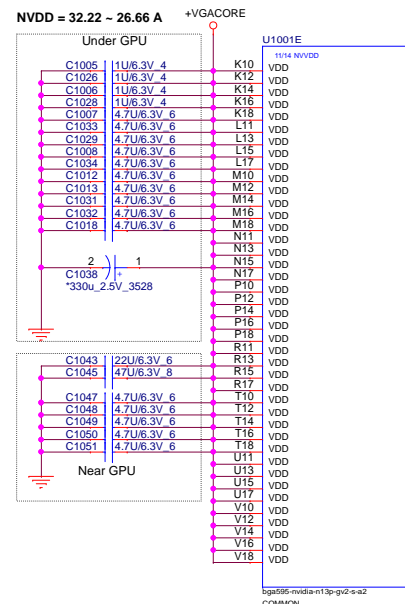
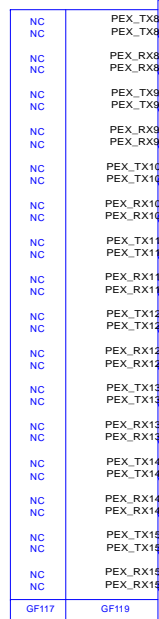
**PEX\_PLLVDD and PEX\_LLVDVDD:** Connected to AA14 and AA15. Note: Near GPU 4.7U/6.3V/6 C1057, 1U/6.3V/4 C1058, 0.1U/16V/4 C1059. Under GPU.

**TESTMODE:** Connected to AD9. Note: 10K/F/4 R1010.

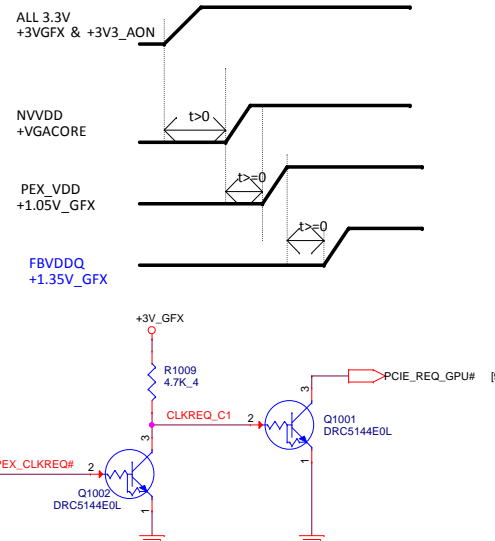
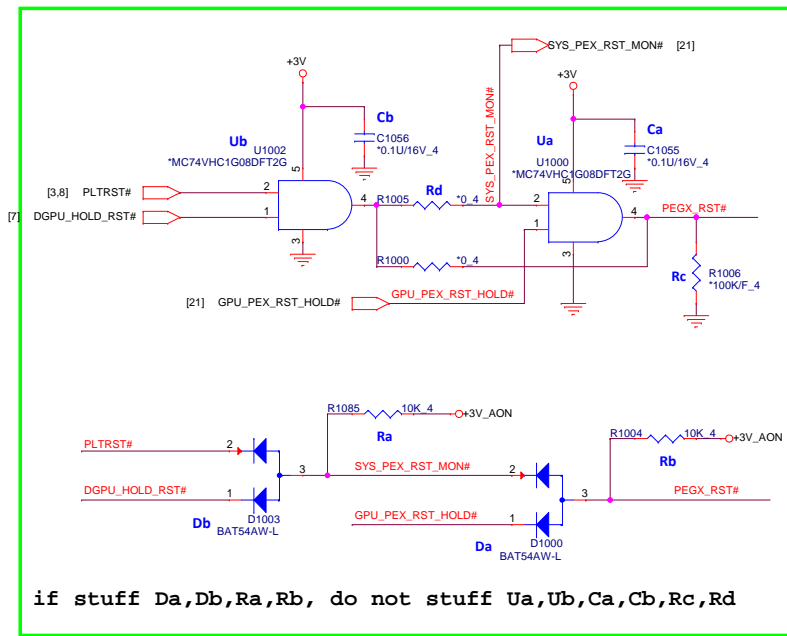
**PEX\_TERM:** Connected to AF25. Note: 2.49K/F/4 R1011.

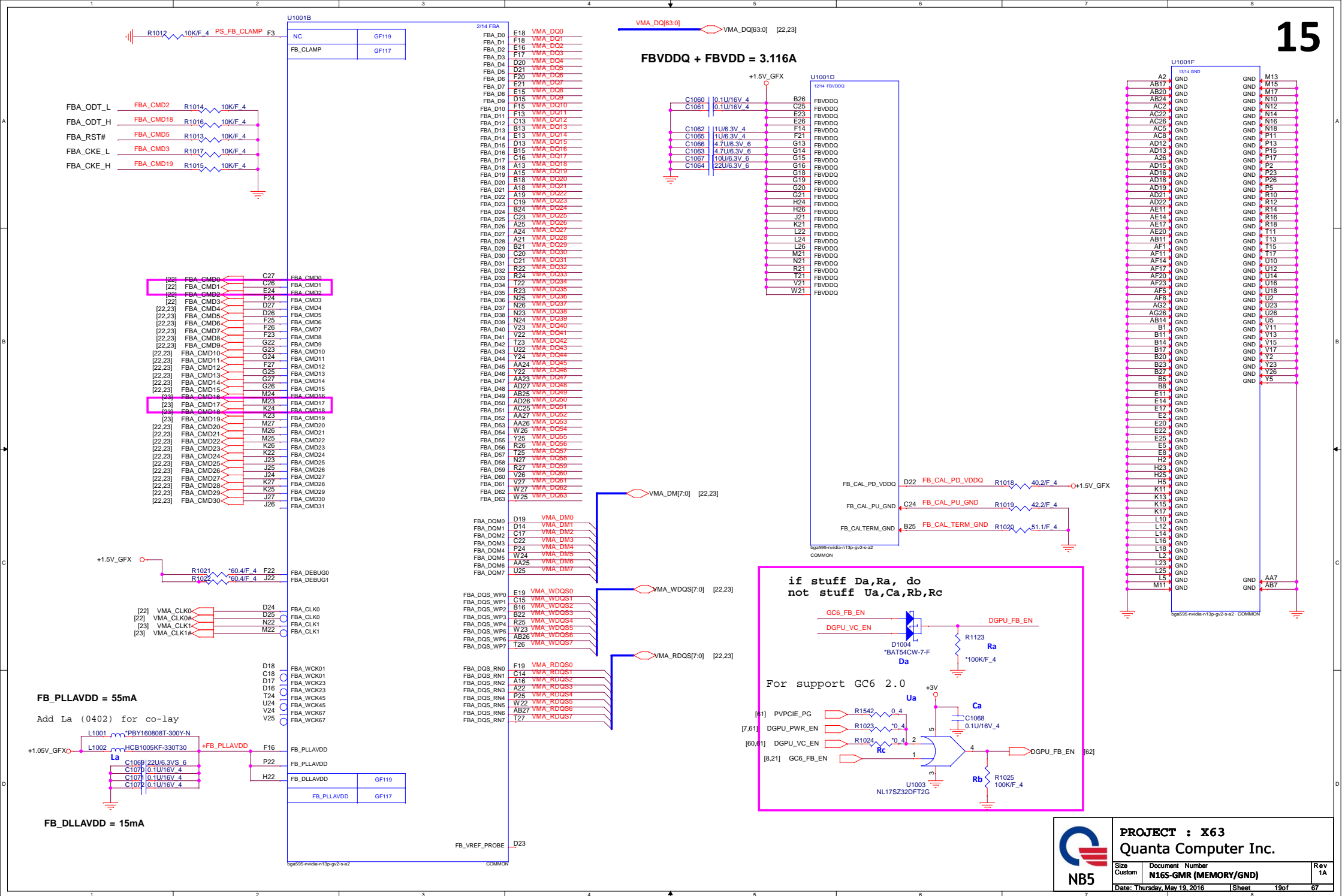
**Power Supply:** +1.05V\_GFX.

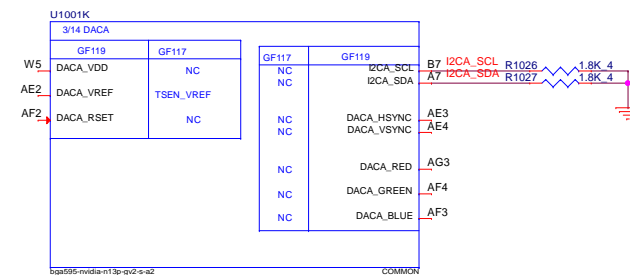
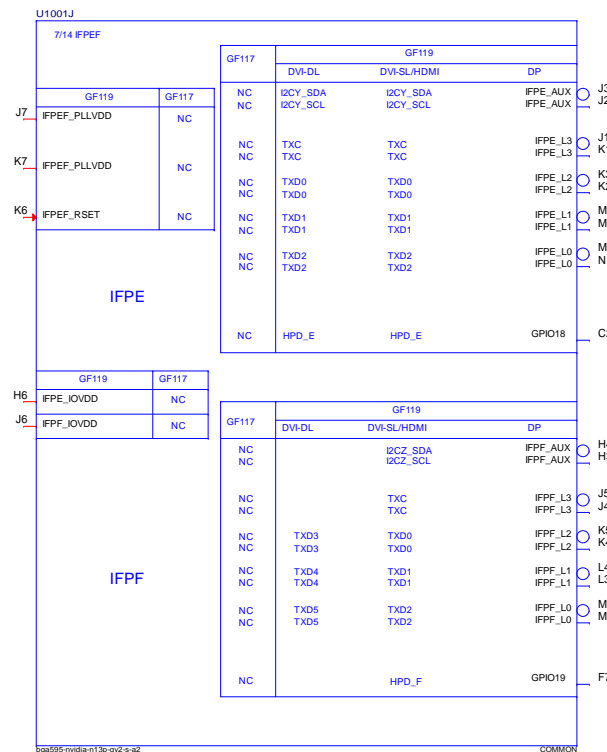
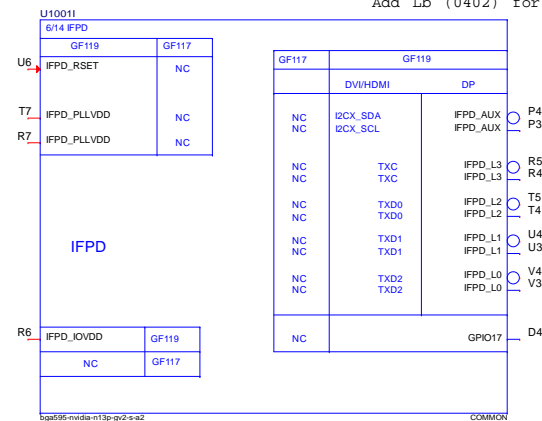
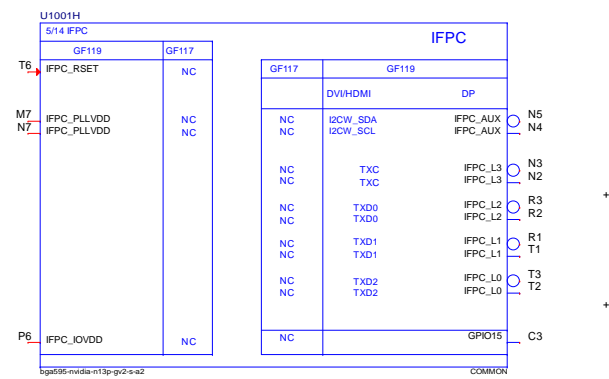
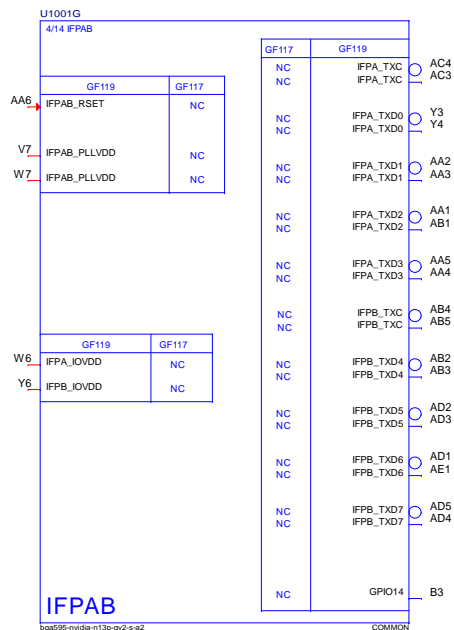
**PEX PLLVDD = 130mA**



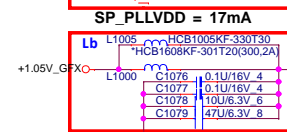
## Power up sequence



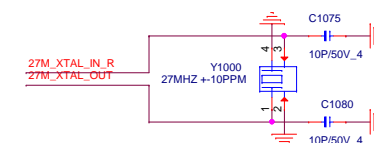
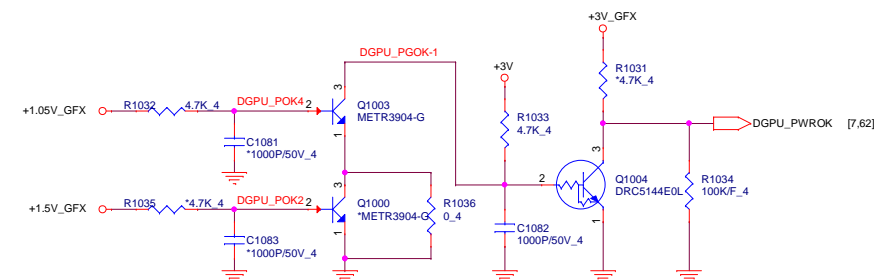




**PLLVD = 38mA** Add La (0402) for co-lay



**VID\_PLLVDD = 41mA**



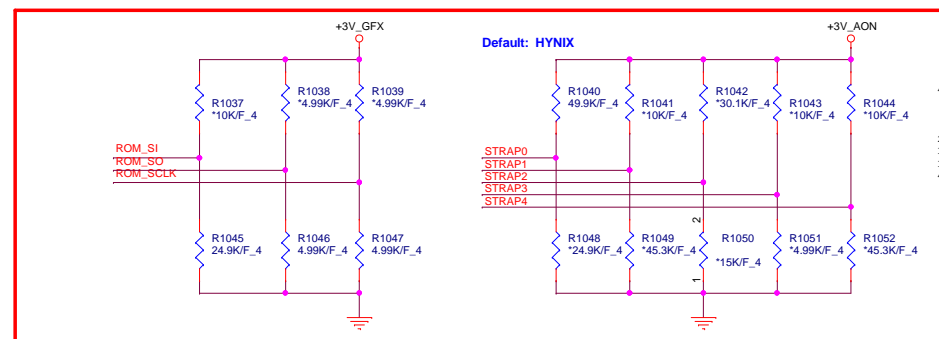
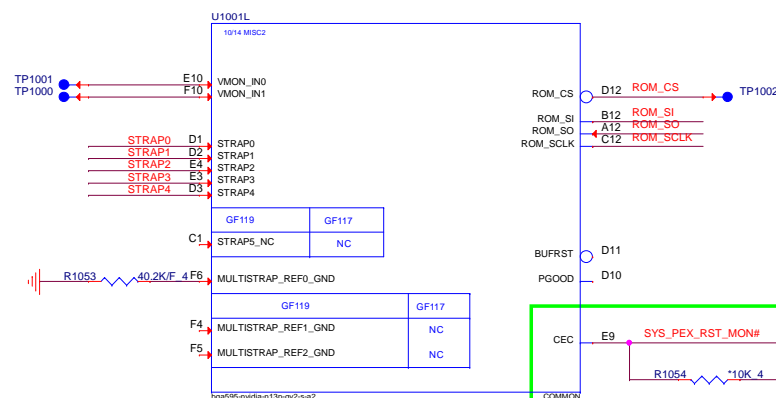
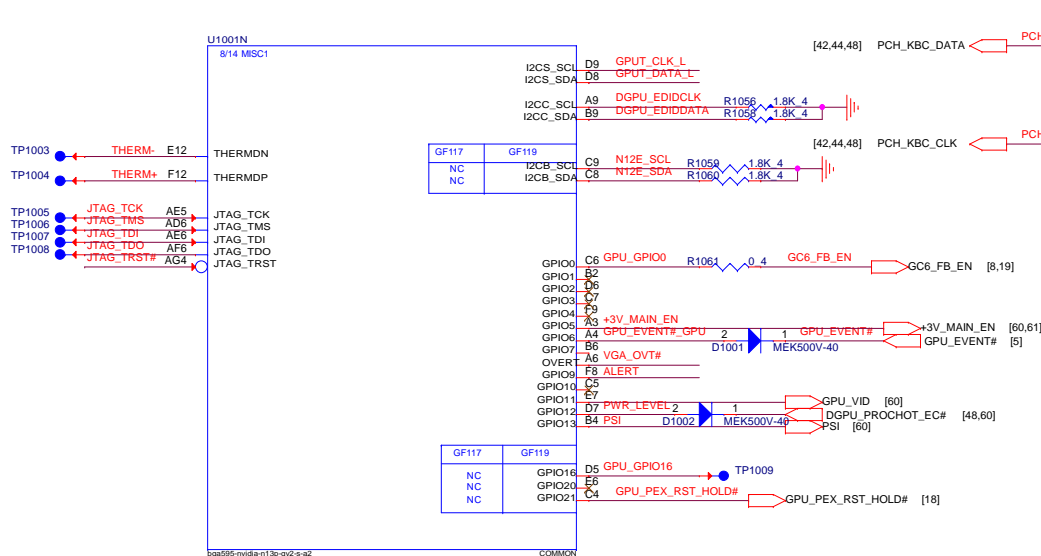


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

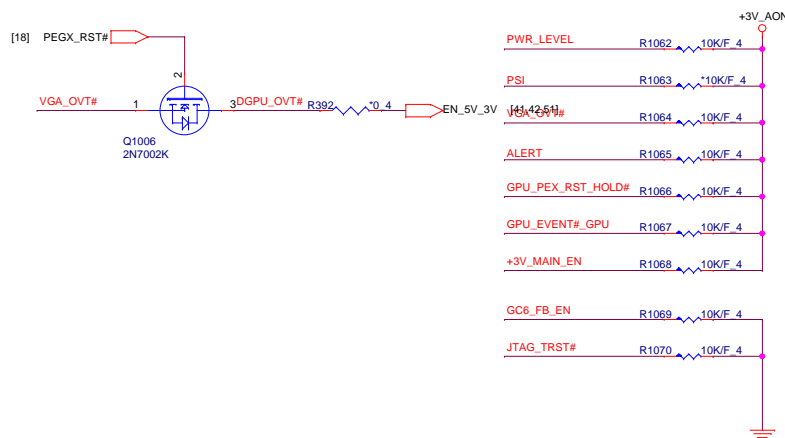


VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59G8T11	AKD59G8T100
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

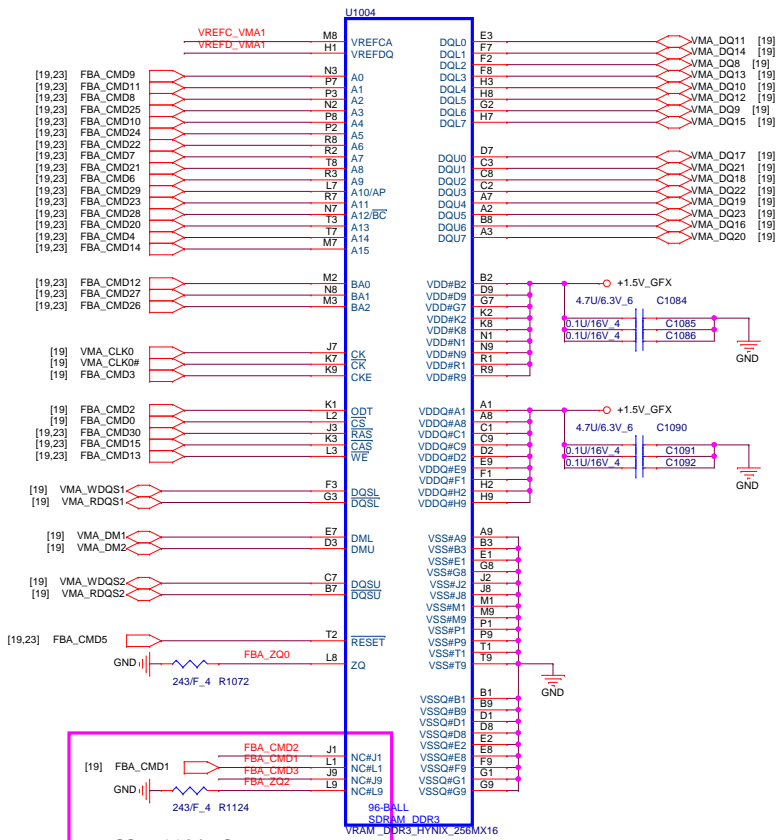


Rank0

```

HYU 256Mx16, H5TC4G63AFR-11C      QBC PN AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E  QBC PN AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A       QBC PN AKD5PGWT501---TOP B/S PN : AKD5PGWT502

```



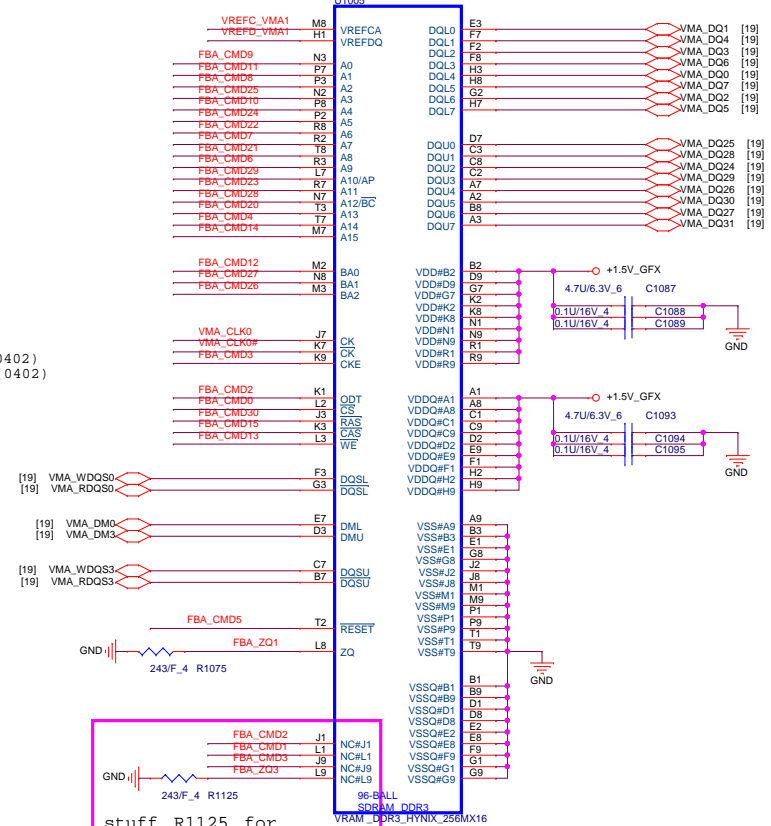
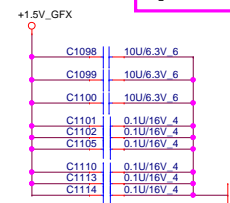
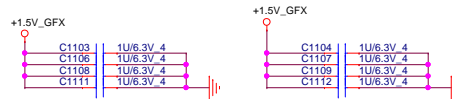
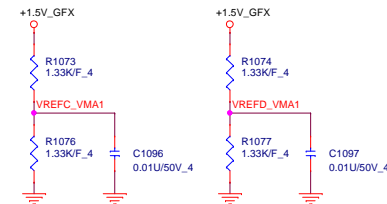
stuff R1124 for  
Hynix 8Gb DDP VRAM

```
reserve for Hynix 8Gb DDP VRAM
```

SDDR3\_BGA100

	0.31	32.63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN FBAO ODT1	J1	NC/ODT1
SNN FBAO CKE1	J9	NC/CKE1
SNN FBAO CS1	L1	NC/CS1
SNN FBAO ZQ1	L9	NC/ZQ1



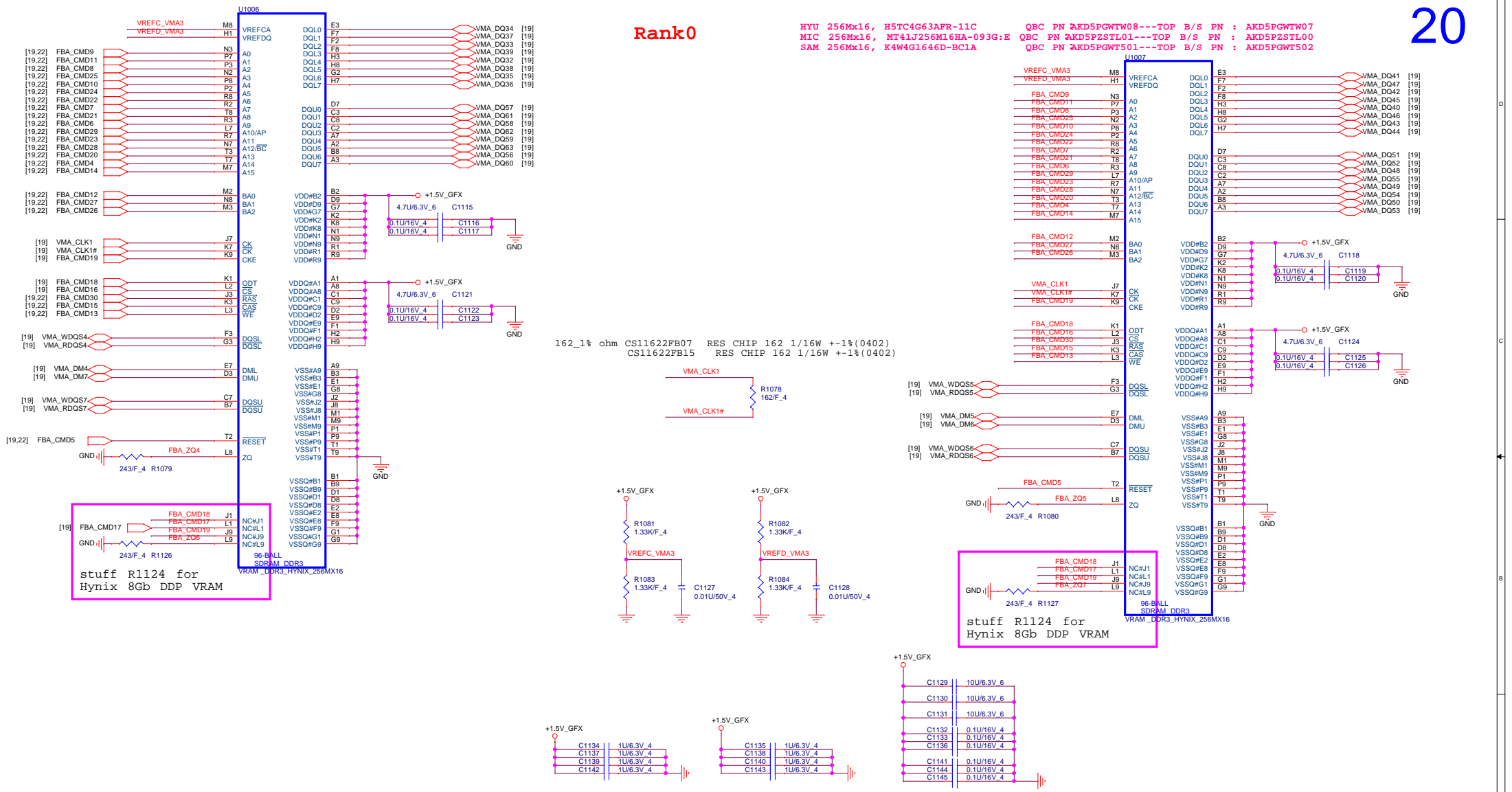
```
stuff R1125 for
Hynix 8Gb DDP VRAM
```



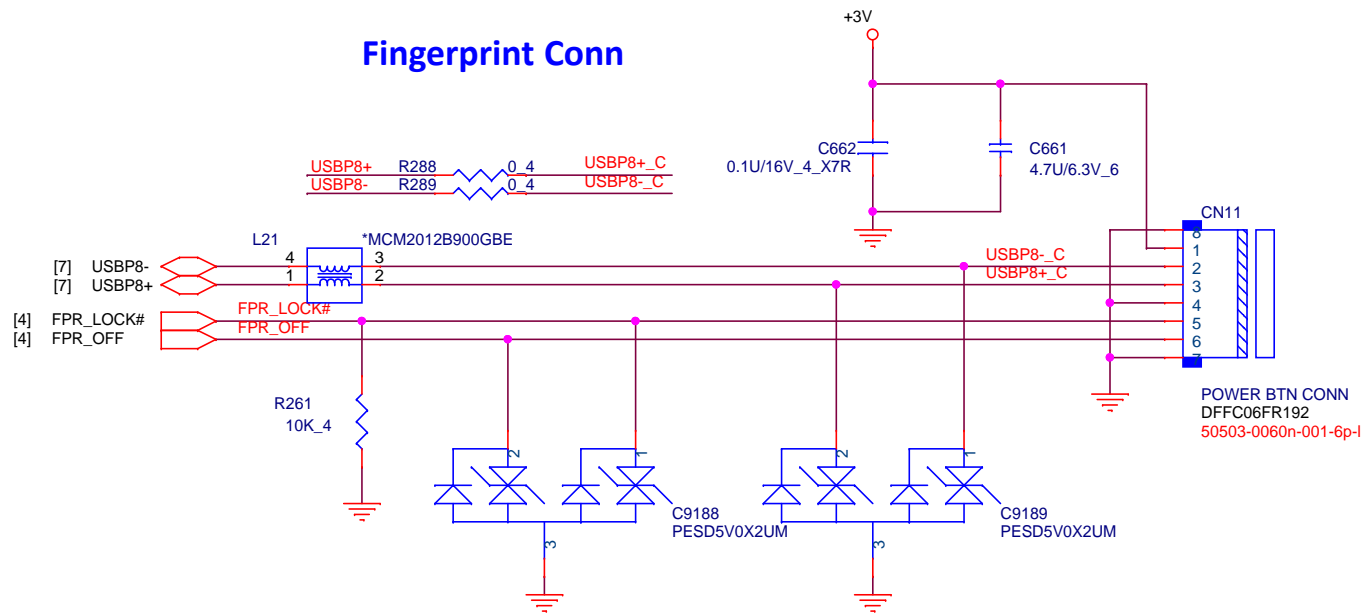
Rank0

HYU 256Mx16, H5TC4G63APR-11C  
MIC 256Mx16, MT41J256M16HA-093G:E  
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
QBC PN AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
QBC PN AKD5PGWT501---TOP B/S PN : AKD5PGWT502



## Fingerprint Conn



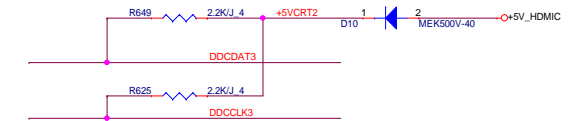
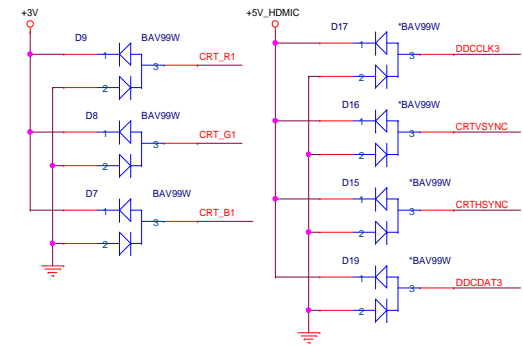
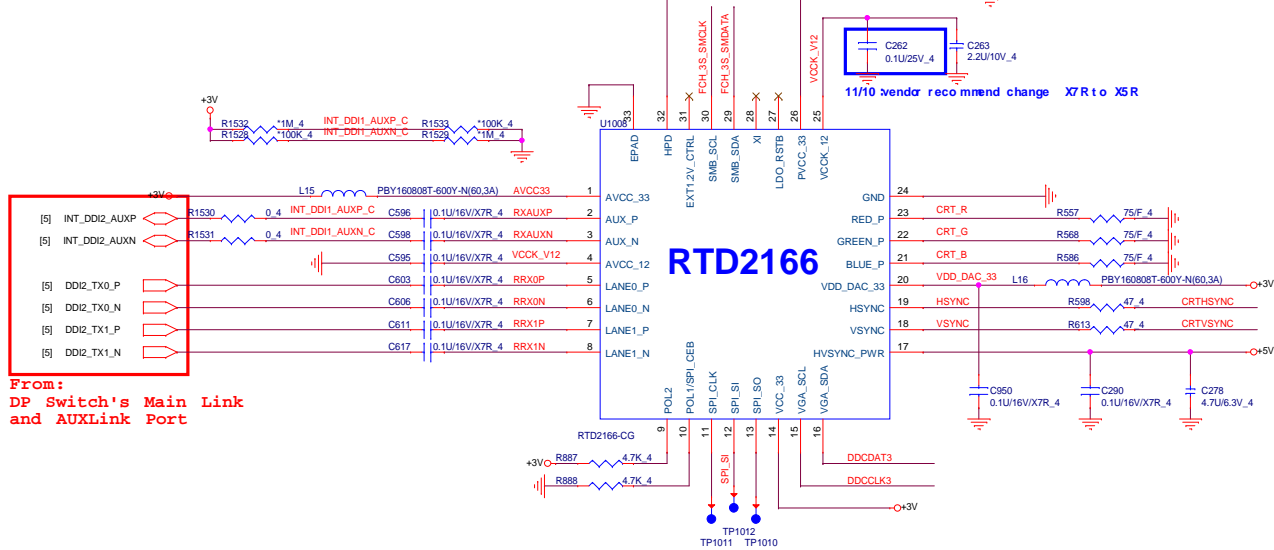


ALF@1119:  
HP confir med to re move the eDP to LVDS convert α.

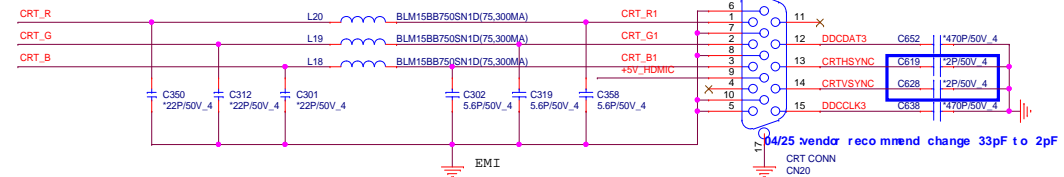
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V



To:  
DP Switch's HPD Input Port  
[5] DDI\_HPD\_CON  
Pull down at SOC side



40 MIL  
C676 0.1u/16V 4 X7R  
SSM14 spec is 40V 1A



Need check footprint and PN

DFDS15FR456  
dsb-10556-15002-15p

### FCH\_3S\_SMCLK, FCH\_3S\_SMDATA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS  
ROM or EEPROM mode: connect to PCH SMBUS  
IIC Protocol is used

**RTD2168 Slave Address:**  
0x64/0x65 and 0x68/0x69

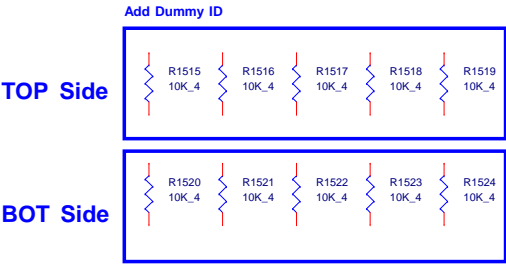
From PCH




**PROJECT : X63**  
**Quanta Computer Inc.**

Size Custom	Document Number 27 - DP2VGA_converter	Rev 1A
Date: Thursday, May 19, 2016	Sheet 27 of 67	

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V <sub>DD</sub>	2 dB
short to V <sub>DD</sub>	short to GND	4 dB
short to V <sub>DD</sub>	short to V <sub>DD</sub>	6 dB



OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



**PROJECT : X63**

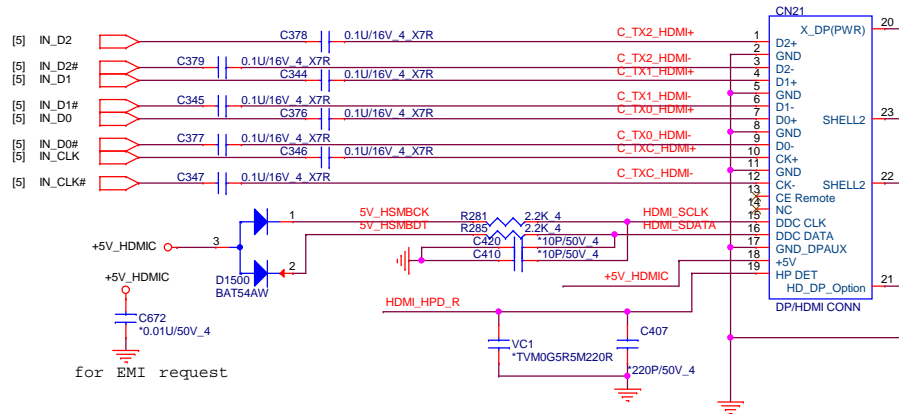
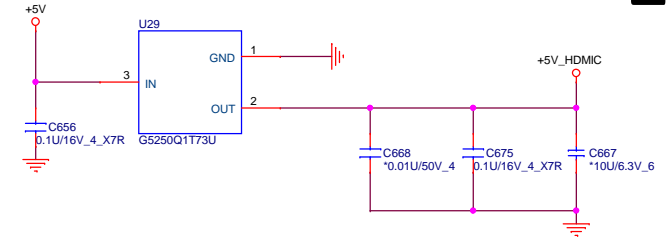
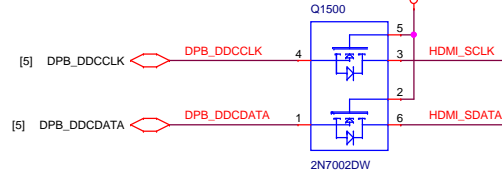
**Quanta Computer Inc.**

Size Custom	Document Number <b>28 – REPEATER PTN3366</b>	Rev 1A
Date: Thursday, May 19, 2016		Sheet 28 of 67

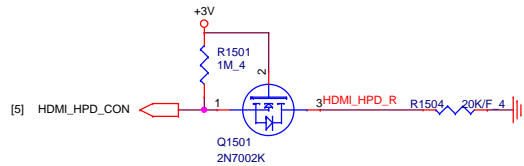
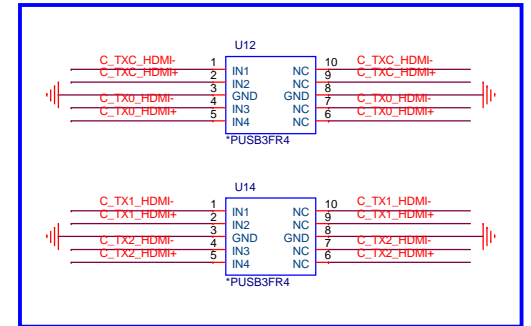
## EMI Solut i on

C_TX2_HDMI+	R304	150/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R291	150/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R295	150/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R299	150/F 4	C_TXC_HDMI-

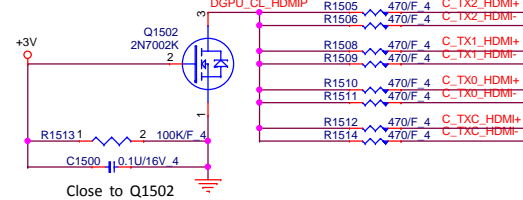
## HDMI SMBus Isol at i on



for EMI request



## Close to HDMI connector

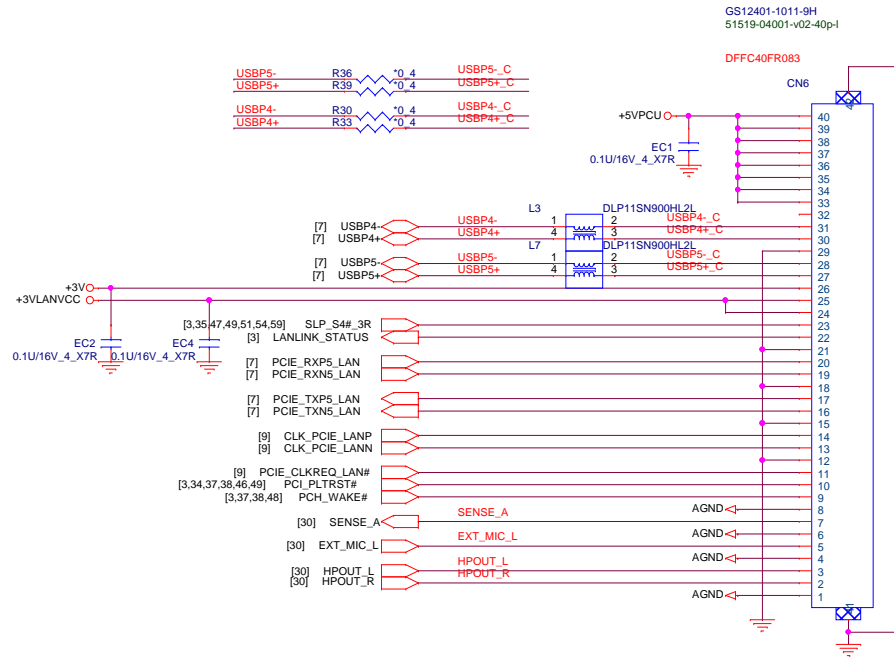



PROJECT : X63  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
29 -- HDMI CONNECTOR		
Date: Thursday, May 19, 2016	Sheet 29 of 67	



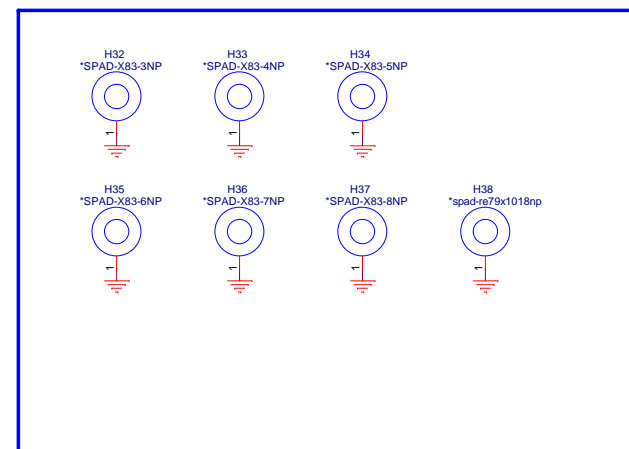
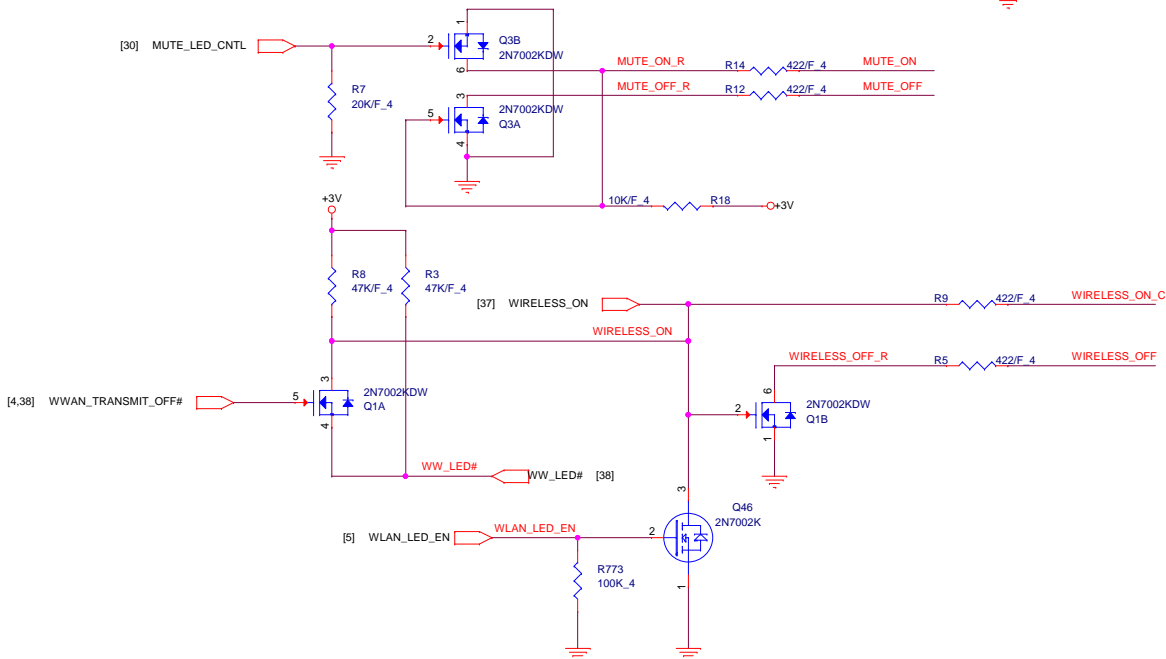
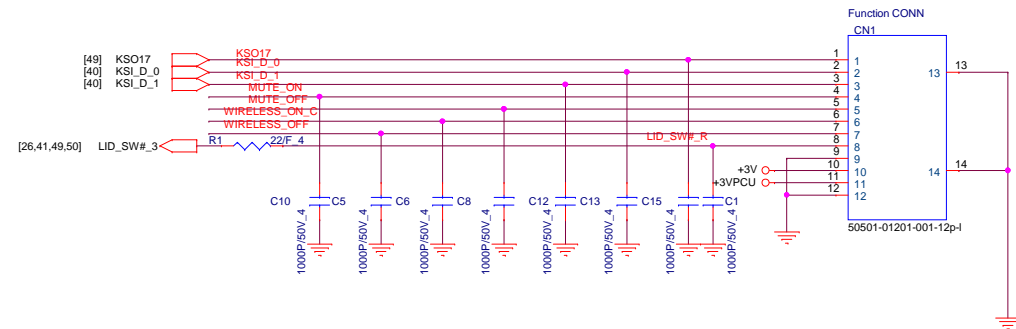
# USB2.0 x2/LAN/Headphone\_Mic Combo Jack Daugther Board Connector



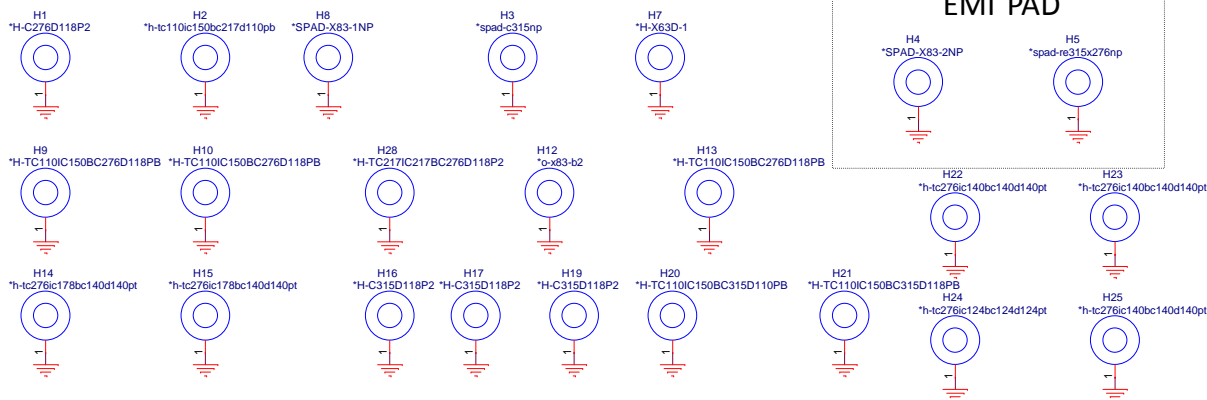
	<b>PROJECT : X63</b>		
	<b>Quanta Computer Inc.</b>		
	Size Custom	Document Number 31 -- DAUGHTER BOARD CONN.	Rev 1A
Date: Thursday, May 19, 2016		Sheet 31 of 67	



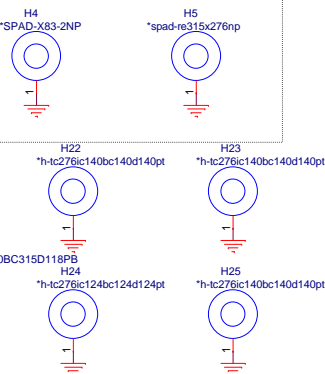




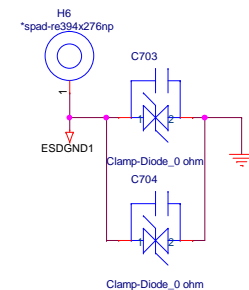
## Hole



## EMI PAD



## ESD PAD



**Hole**

H1: \*H-C276D118P2

H2: \*h-tc110ic150bc217d110pb

H8: \*SPAD-X83-1NP

H3: \*spad-c315np

H7: \*H-X63D-1

H9: \*H-TC110IC150BC276D118PB

H10: \*H-TC110IC150BC276D118PB

H28: \*H-TC217IC217BC276D118P2

H12: \*o-x83-b2

H13: \*H-TC110IC150BC276D118PB

H14: \*h-tc276ic178bc140d140pt

H15: \*h-tc276ic178bc140d140pt

H16: \*H-C315D118P2

H17: \*H-C315D118P2

H19: \*H-C315D118P2

H20: \*H-TC110IC150BC315D110PB

H21: \*H-TC110IC150BC315D118PB

H22: \*h-tc276ic140bc140d140pt

H23: \*h-tc276ic140bc140d140pt

H24: \*h-tc276ic124bc124d124pt

H25: \*h-tc276ic140bc140d140pt

**EMI PAD**

H4: \*SPAD-X83-2NP

H5: \*spad-re315x276np

H22: \*h-tc276ic140bc140d140pt

H23: \*h-tc276ic140bc140d140pt

H24: \*h-tc276ic124bc124d124pt

H25: \*h-tc276ic140bc140d140pt

**ESD PAD**

H6: \*spad-re394x276np

H26: \*H-TC217IC150BC276D118P2

H27: WLAN Nut BOT

H28: \*spad-x83-b1

H29: \*spad-re12x20np

H30: \*spad-re12x20np

H31: \*spad-re12x20np

**WLAN Nut**

H27: WLAN Nut BOT

**NB5**

**PROJECT : X63**

**Quanta Computer Inc.**

Size: Custom

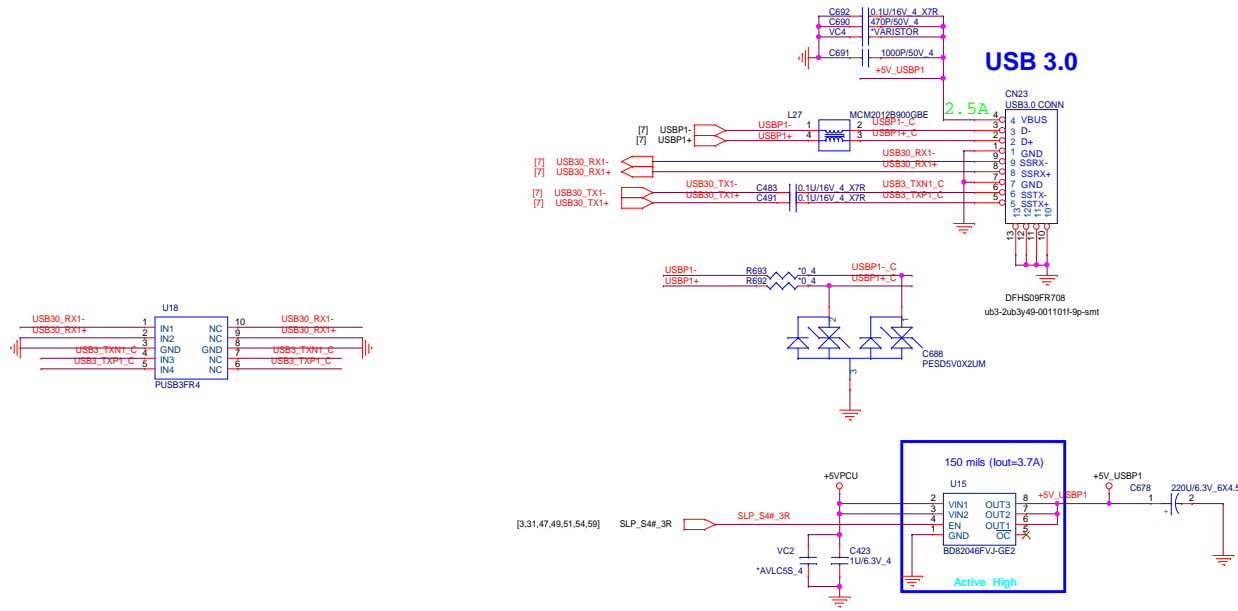
Document Number: 33 - Function Conn./Hole

Date: Thursday, May 19, 2016

Rev: 1A

Sheet: 33 of 67





[31,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67]  
[9,41,51,52,53,59,63,64,67]

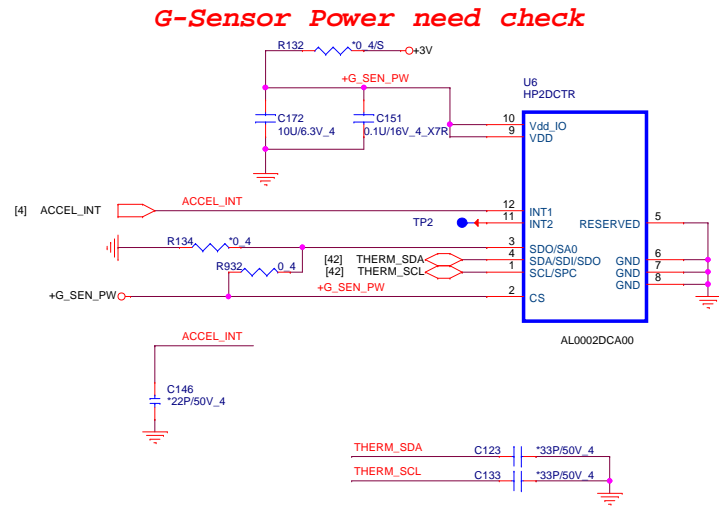
+5VPCU  
+3V\_ALW



PROJECT : X63  
Quanta Computer Inc.

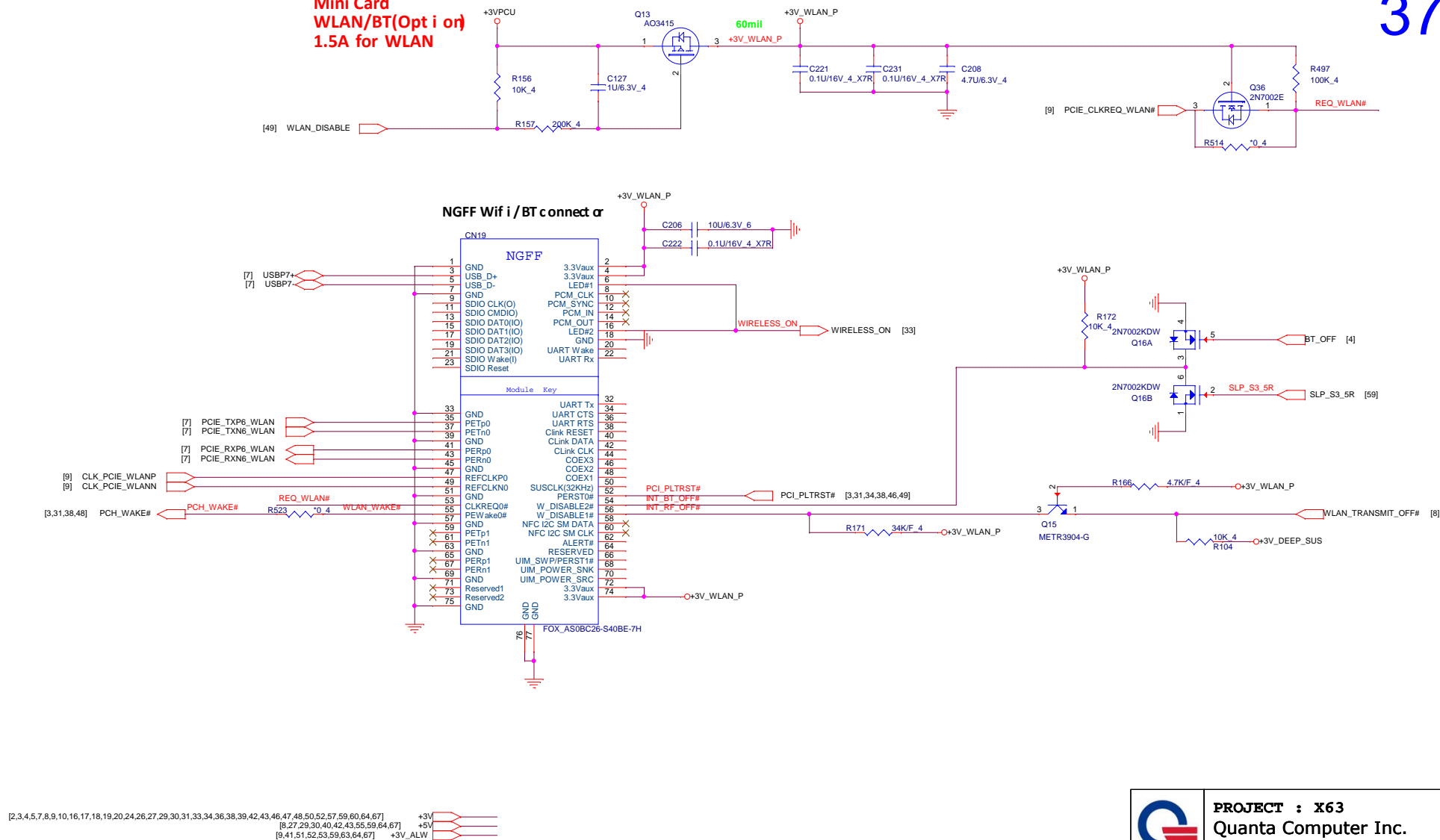
Size Custom	Document Number 35 -- USB3.0 x2	Rev 1A
Date: Thursday, Mar 19, 2016		Sheet 35 of 67


Accelerometer Sensor

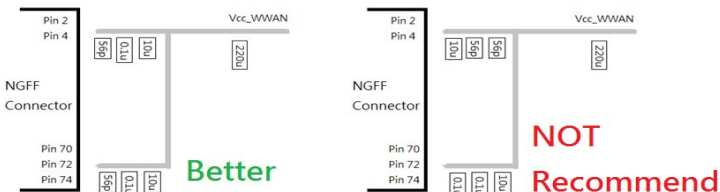


[31,35,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU  
[9,41,51,52,53,59,63,64,67] +3V\_ALW

Mini Card  
WLAN/BT(Optional)  
1.5A for WLAN

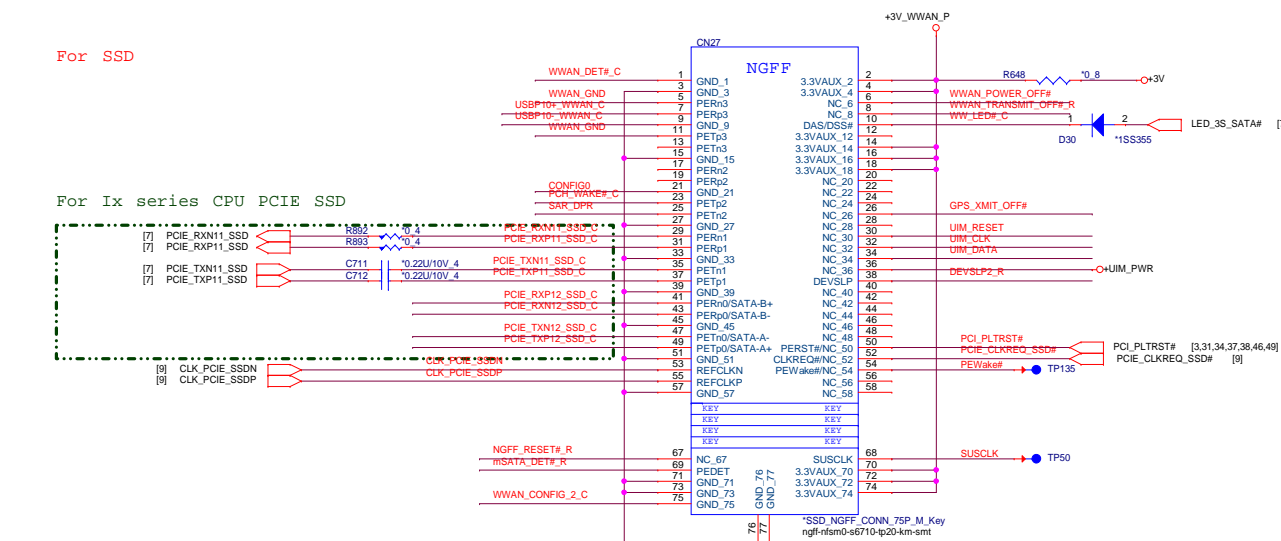


 NB5	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>		
	Size Custom Date: Thursday, May 19, 2016	Document Number <b>37 - NGFF WLAN/BT</b> Sheet 37 of 67	Rev 1A

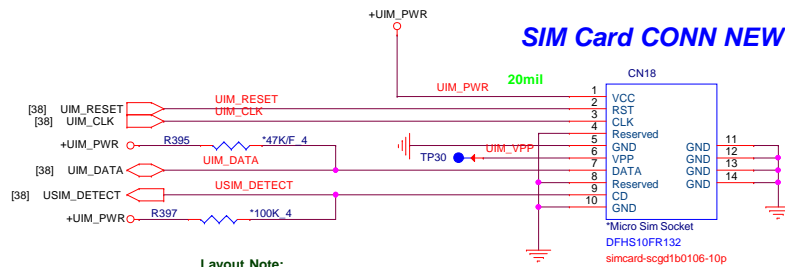


+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

↵	<b>M.2 Pinout</b> ↵	S0↵	S3 – S5↵
WWAN 3.3V↵	2, 4, 70, 72, 74↵	On↵	Off↵

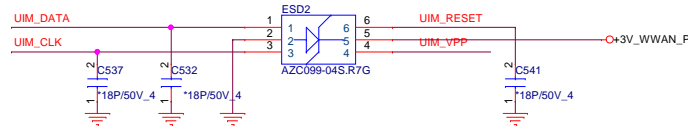
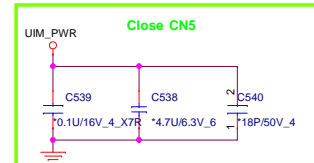


## SIM Card CONN NEW



## Layout Note:

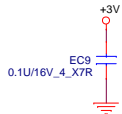
1. UIM\_RESET, UIM\_CLK, UIM\_DATA routing as short as possible. Route into ESD then go out.
2. Avoid routing the SIM\_CLK and SIM\_DATA lines in parallel over distances  $\geq 2$  cm.
3. Position the SIM connector from the WWAN module  $\leq 100$ mm if possible, NOT exceed length is 150mm.

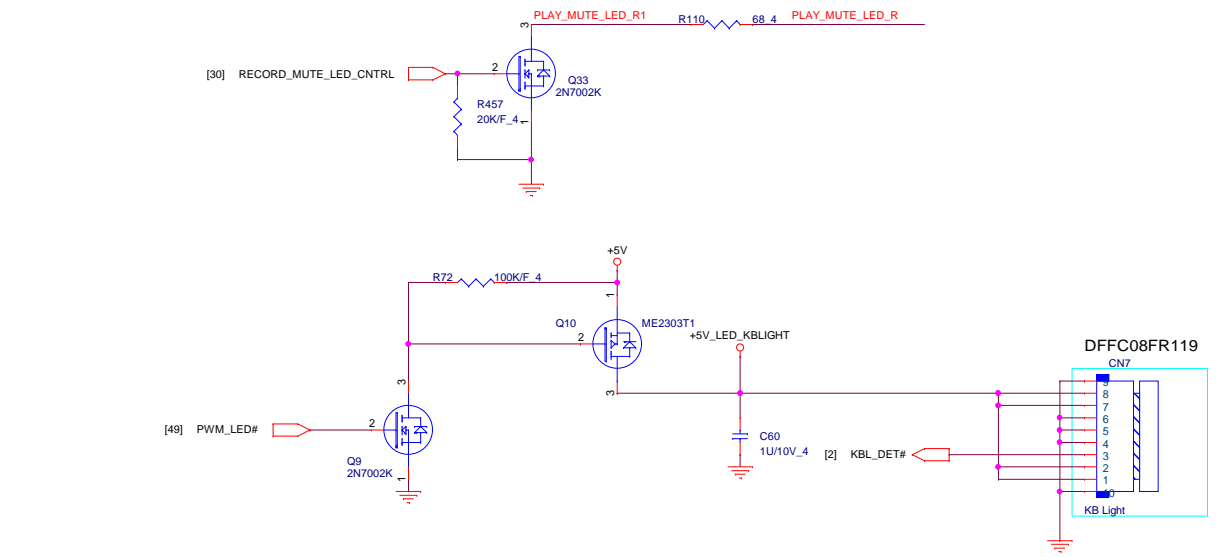
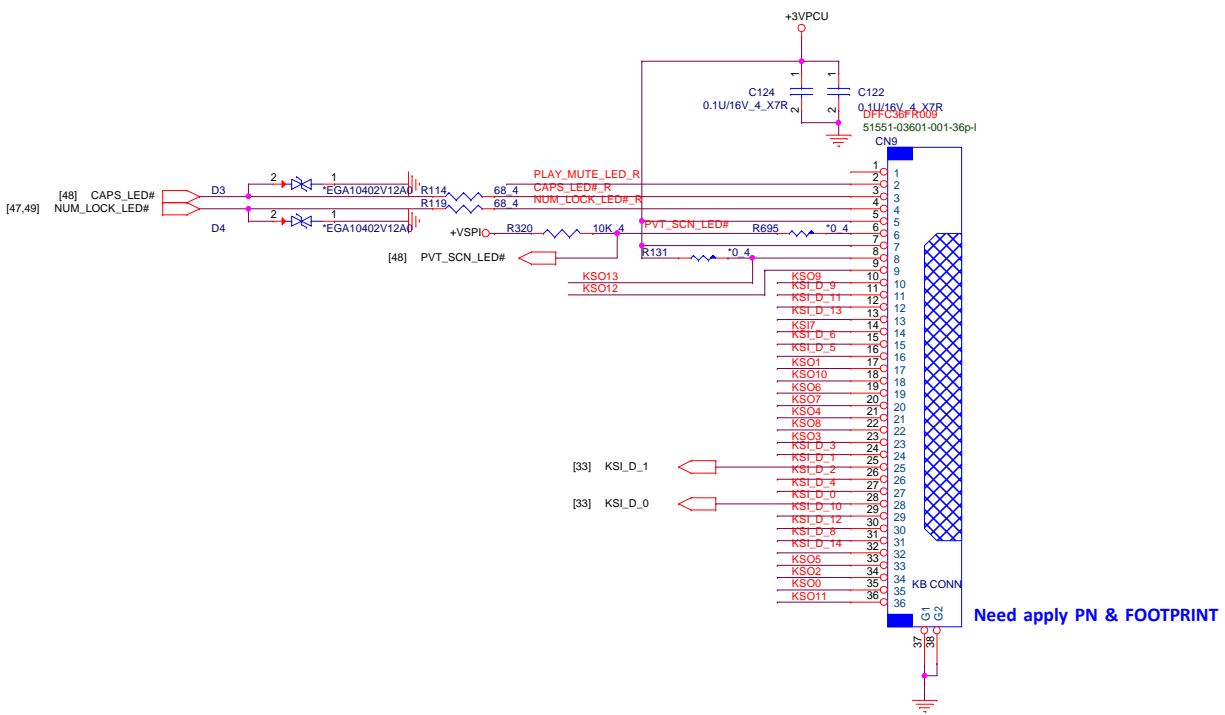
Trace Length and Routing<sup>u</sup>

- Special attention should be paid to SIM traces (UIM\_CLK, UIM\_DATA and UIM\_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.<sup>u</sup>
- Minimum distance between UIM\_CLK and UIM\_DATA should be 20 mils. Static signals such as UIM\_RST can be routed between UIM\_CLK and UIM\_DATA to conserve space if needed.<sup>u</sup>
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM\_CLK, UIM\_DATA and any other high-speed switching signals.<sup>u</sup>
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.<sup>u</sup>

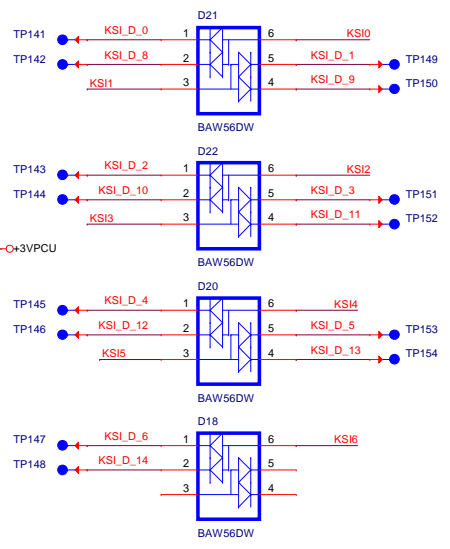
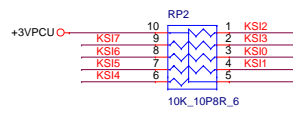
SIM Power<sup>u</sup>

- The UIM\_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.<sup>u</sup>
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM\_PWR supply and locate near the SIM connector.<sup>u</sup>

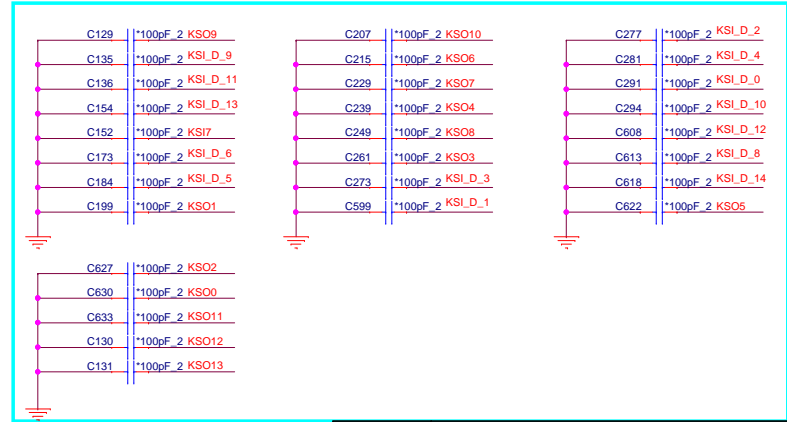




KEYBOARD PULL-UP




For EMI reserved



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]  
[8,27,29,30,42,43,55,59,64,67]  
[9,41,51,52,53,59,63,64,67]

+3V  
+5V  
+3V\_ALW



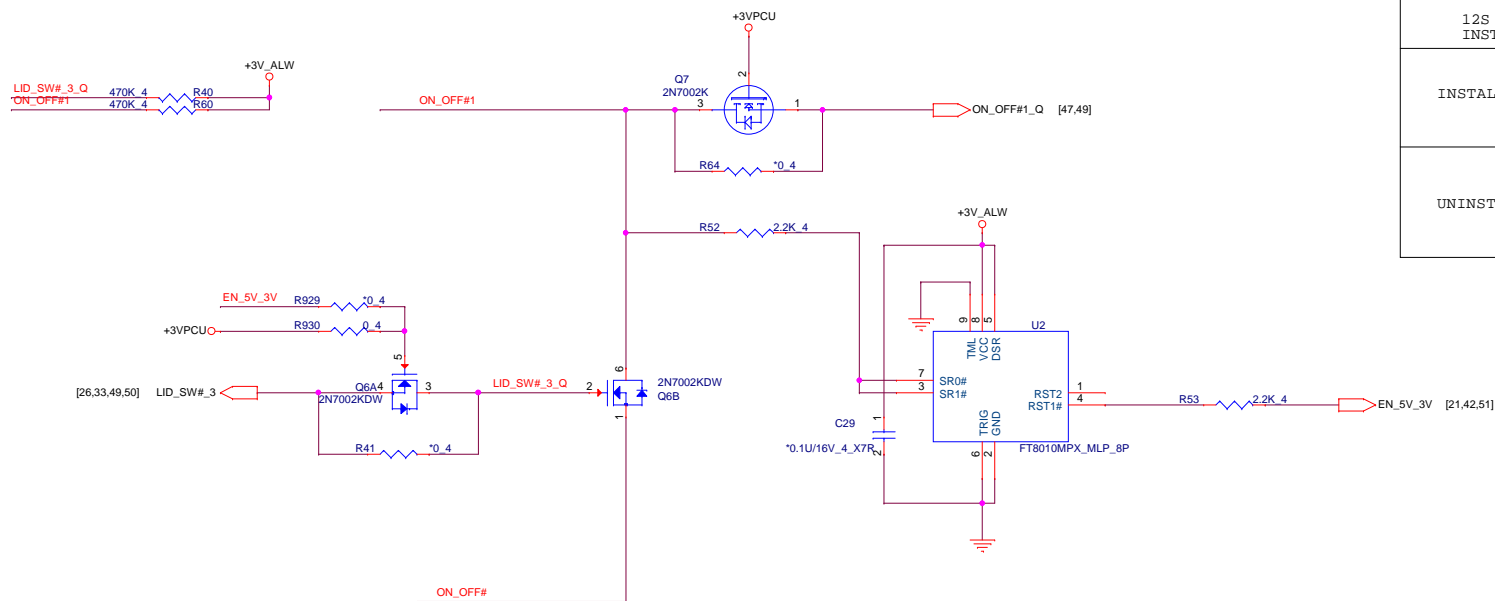
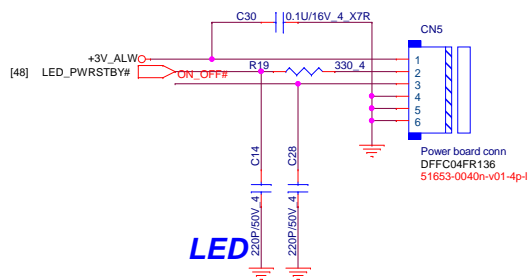
**PROJECT : X63**

**Quanta Computer Inc.**

Size	Document	Number	Rev
Custom	40 -- KB/ KB light CONN		1A
Date: Thursday, May 19, 2016		Sheet 40 of 67	



Power Button on Connector

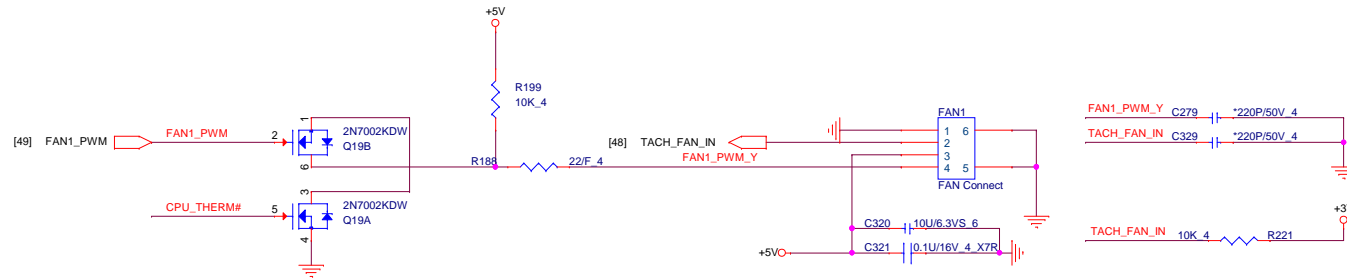


12S RESET MODE INSTAL FOR DB0		
INSTAL	R10702 R10704 R10701 U9068	R10703 R? R? Q7081
UNINSTAL	R? Q7080	R? Q7081

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V  
[8,27,29,30,40,42,43,55,59,64,67] +5V  
[9,51,52,53,59,63,64,67] +3V\_ALW

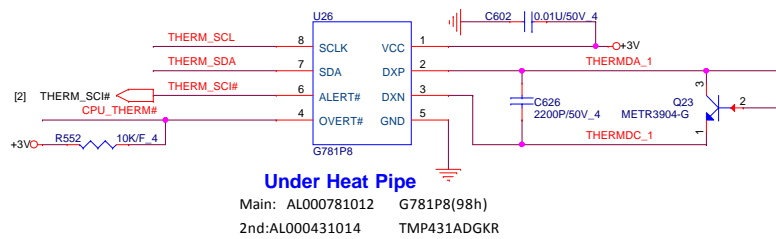
**PROJECT : X63**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>41 - Power Button/ HW Reset</b>	Rev 1A
Date: Thursday, May 19, 2016	Sheet 41 of 67	

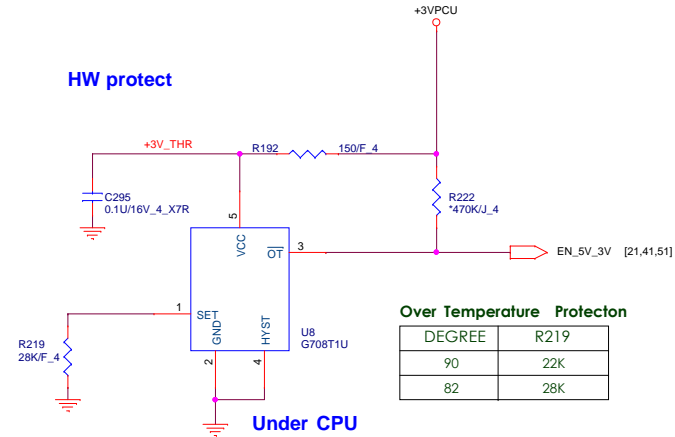


## Thermal sensor

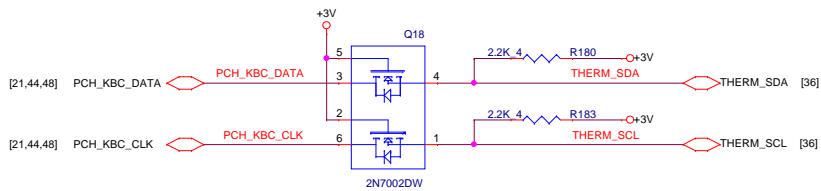
### CPU Thermal Sensor



### HW protect



$$RSET \text{ (K OHM)} = 0.0012T^2 - 0.9308T + 96.147$$



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,43,46,47,48,50,52,57,59,60,64,67]  
[9,41,51,52,53,59,63,64,67]

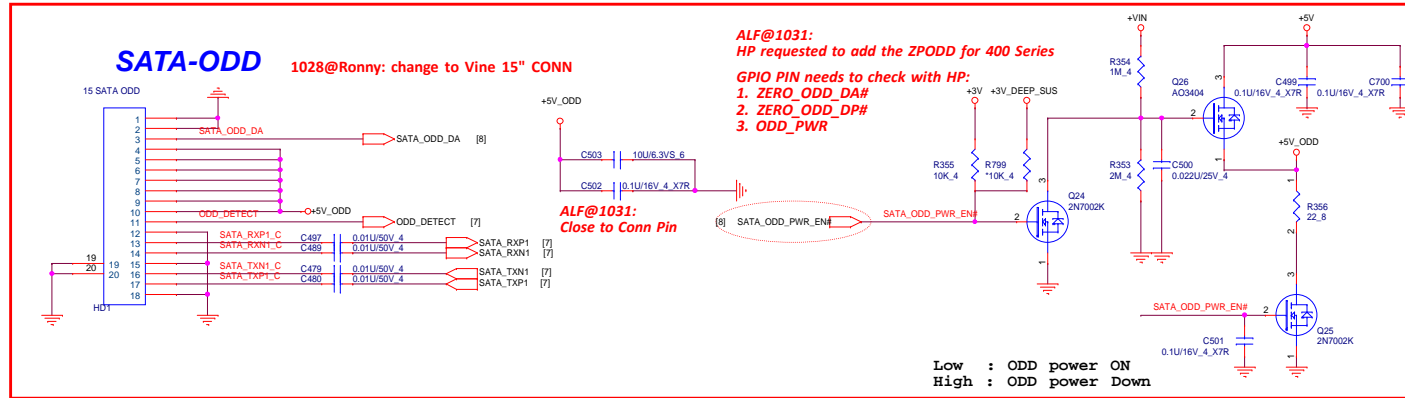
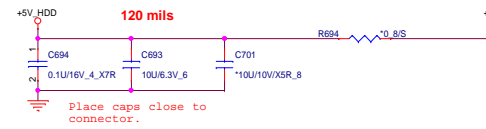
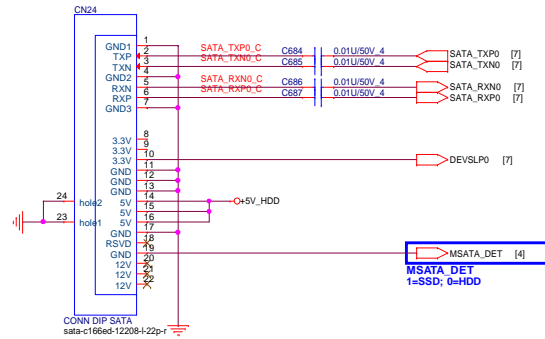
+3V  
+3V\_ALW



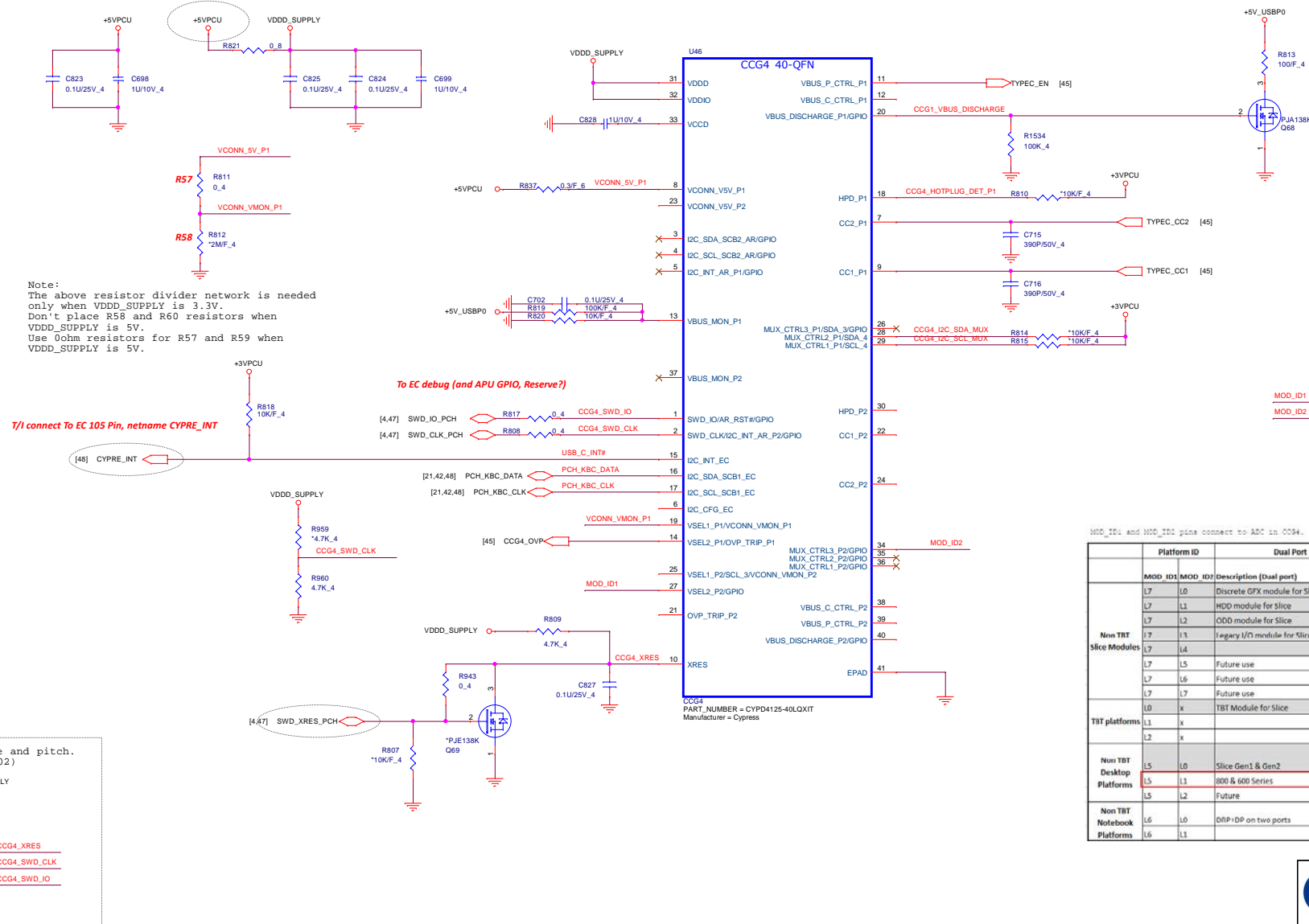
PROJECT : X63  
Quanta Computer Inc.

Size Custom	Document Number 42-- FAN and Thermal IC	Rev 1A
Date: Thursday, May 19, 2016	Sheet 42 of 67	

## SATA-HDD



SI, 2/23, Change 5V



MOD\_ID1 and MOD\_ID2 pins connect to ADC in CCG4.

	Platform ID	Dual Port	Dual Port	Single Port	Single Port
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (single)	CFGID
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0	CFG0
	L7	L1	HDD module for Slice	CFG1	CFG1
	L7	L2	ODD module for Slice	CFG1	CFG1
	L7	L3	Legacy I/O module for Slice	CFG1	CFG1
	L7	L4	Future use	Communication	CFG0
	L7	L5	Future use		
	L7	L6	Future use		
TBT platforms	L0	x	TBT Module for Slice	CFG2	CFG2
	L1	x		Slice Gen2	CFG1
Non TBT Desktop Platforms	L5	L0	Slice Gen1 & Gen2	CFG3	CFG3
	L5	L1	800 & 600 Series	CFG4	800 & 600 Series (DPP) CFG4
	L5	L2	Future	800 & 600 (DPP+DP)	CFG5
Non TBT Notebook Platforms	L6	L0	DRP+DP on two ports	CFG5	CFG4
	L6	L1	Future	DRP+DP on single port	CFG5



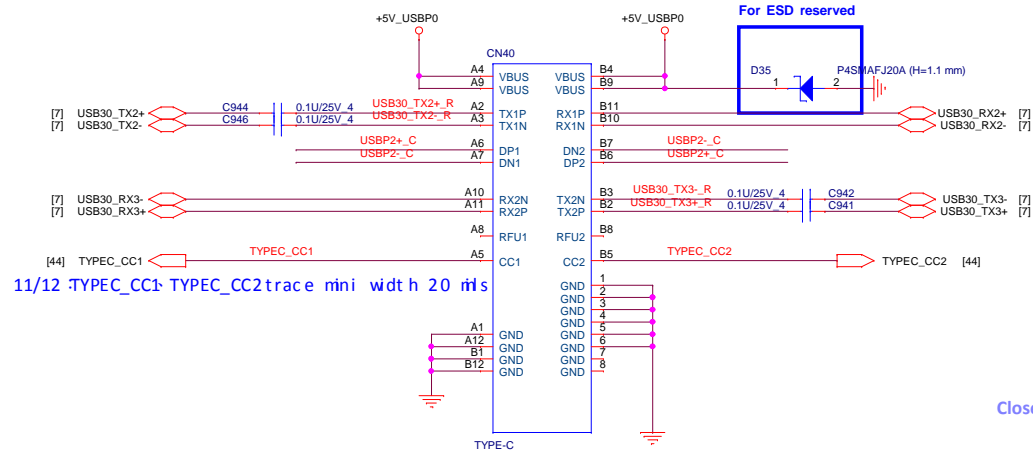
**PROJECT:400 Series**  
**Quanta Computer Inc.**

Size Document Number  
**44 - Cypress CCG4**

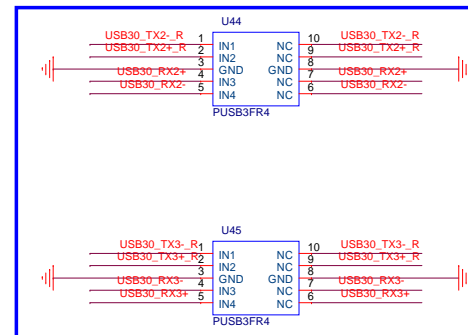
Date: Thursday, May 19, 2016 Sheet 44 of 67

NB5

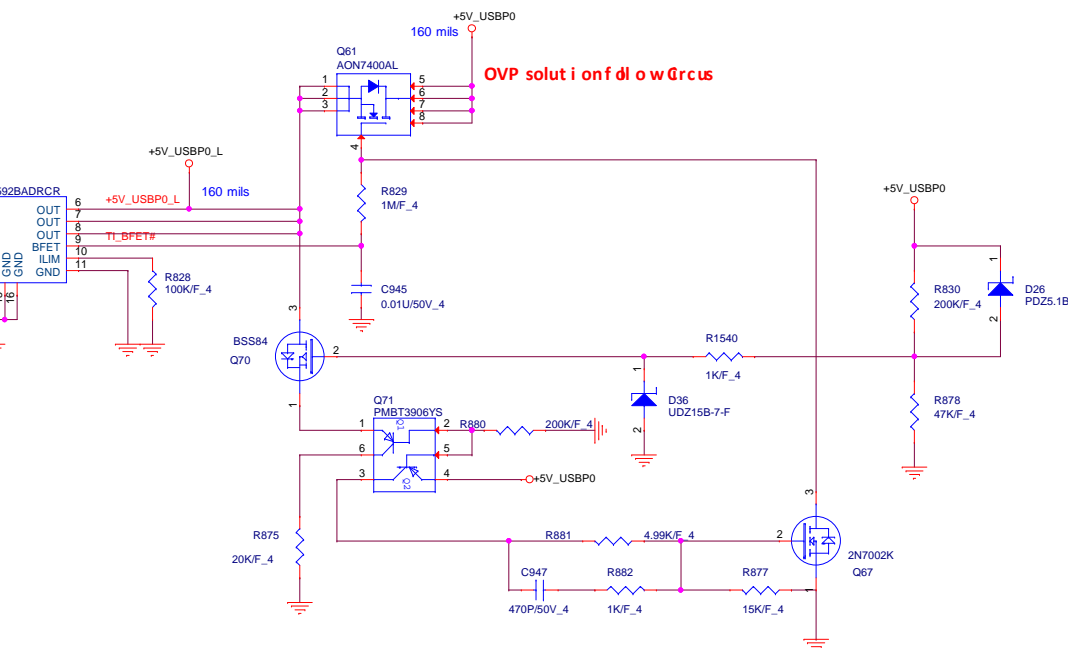
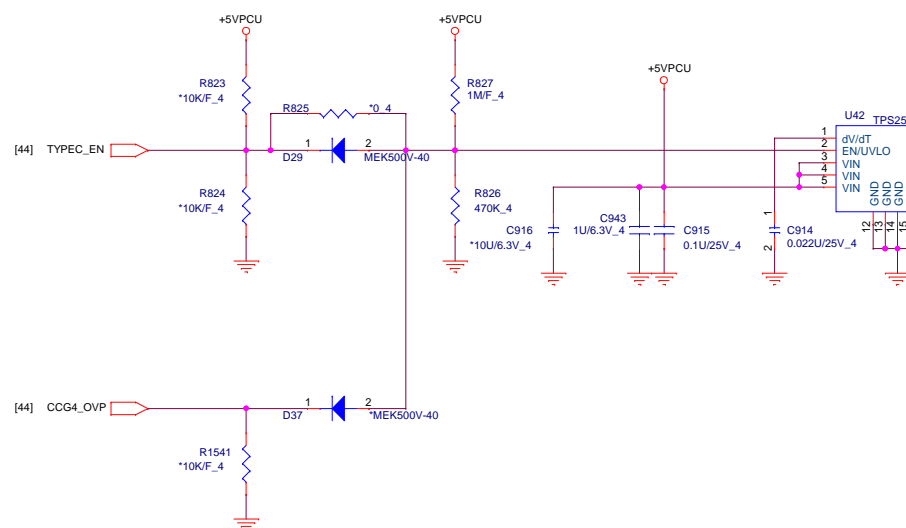
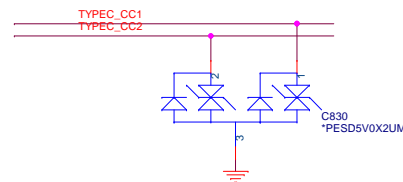
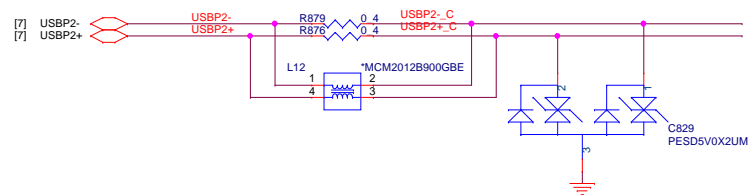
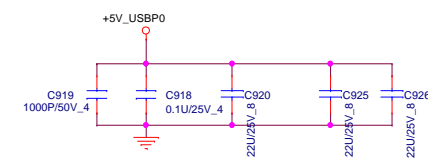
Rev 1A



## Reserve ESD chip



## Close CN40

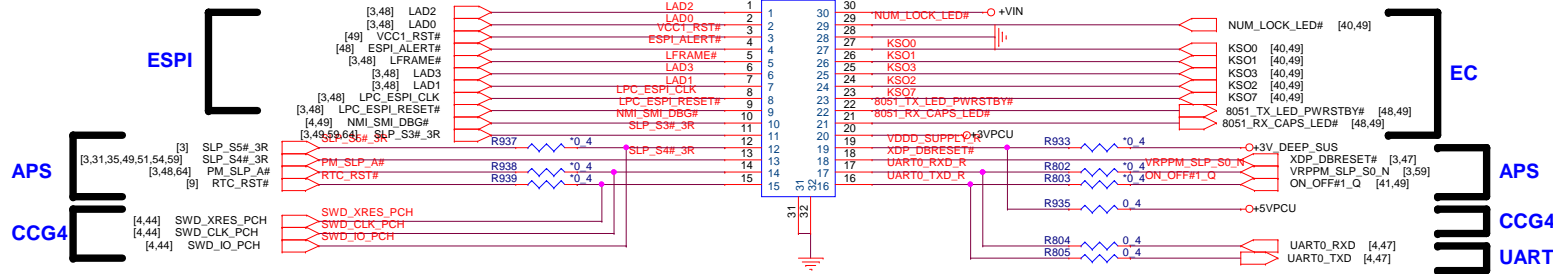




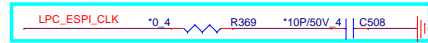
# ESPI+EC+APS debug conn on MB

debug\_CONN\_30P

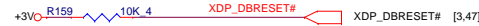
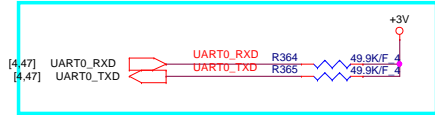
CN14



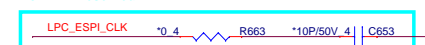
For EMI reserved



For check list



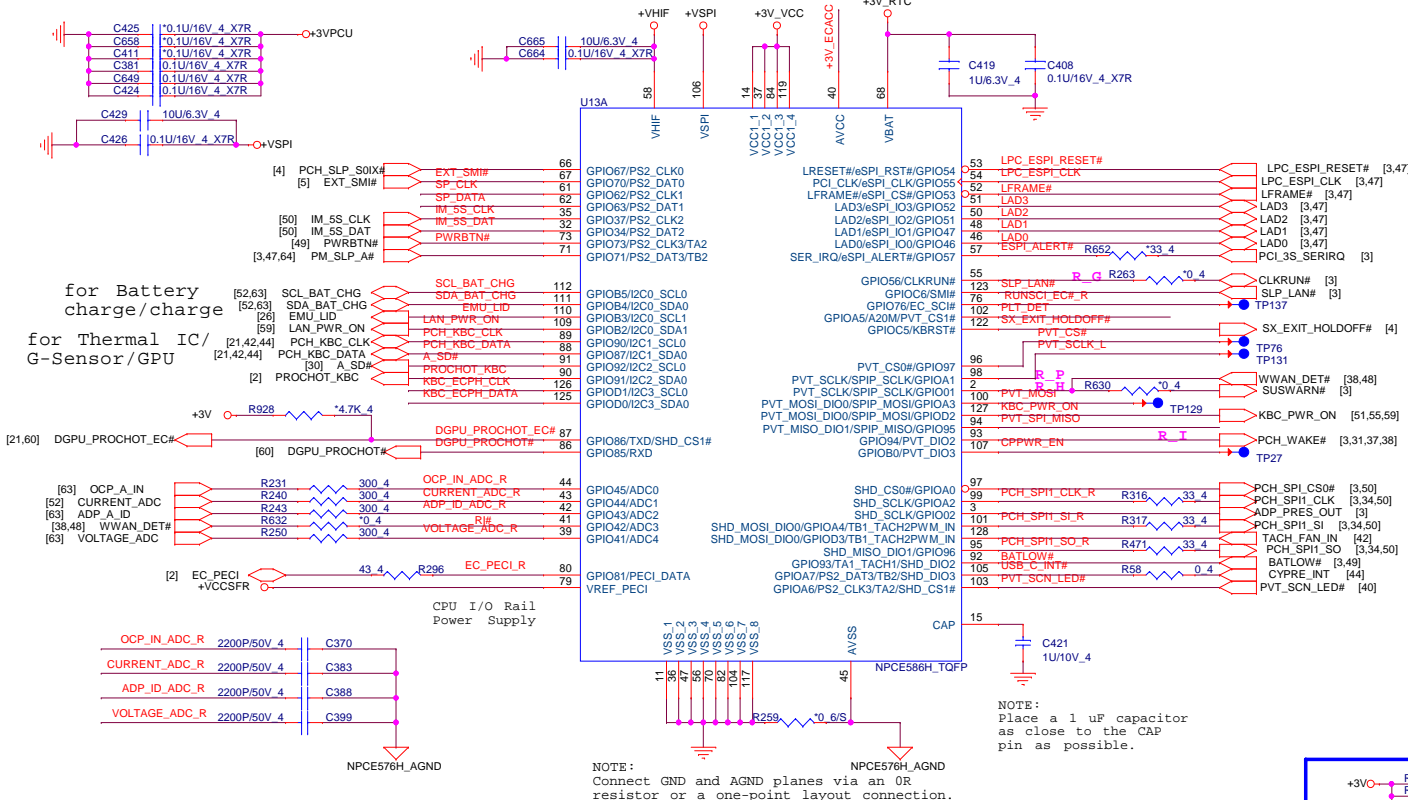
For EMI reserved



	eSPI Mode	LPC Mode
R263 <b>R_G</b>	Un-Install	Install
R630 <b>R_H</b>	Un-Install	Install
R307 <b>R_I</b>	Un-Install	Install
R631 <b>R_P</b>	Install	Un-Install

for Battery  
charge/charge

for Thermal IC/  
G-Sensor/GPU

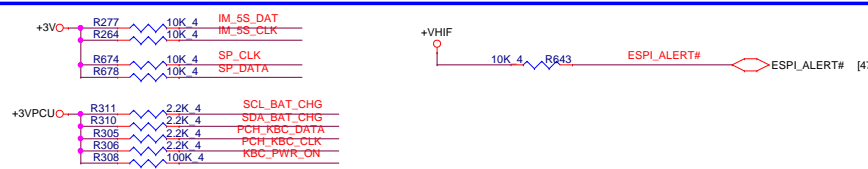
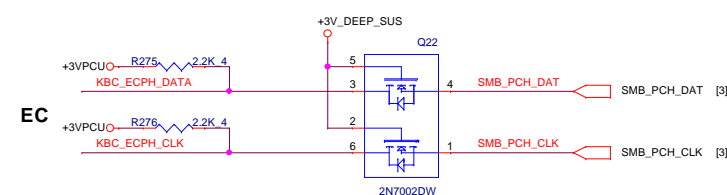


NOTE:  
Place a 1 uF capacitor  
as close to the CAP  
pin as possible.

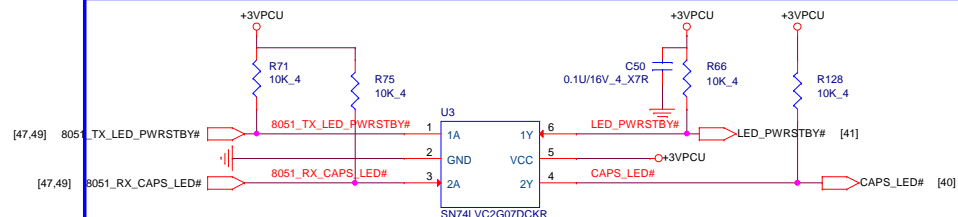
PVT\_SCLK



EC



PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS



**PROJECT : X63**  
**Quanta Computer Inc.**

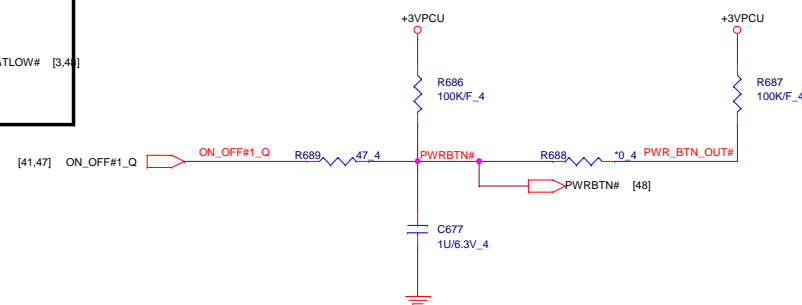
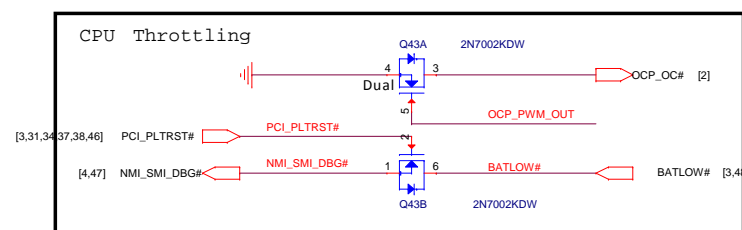
Size	Document Number	Rev
Custom	45 - EC NuvoTon NPCE586H_1	1A
Date: Thursday, May 19, 2016	Sheet 48 of 67	

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,50,52,57,59,60,64,67]  
[9,41,51,52,53,59,63,64,67]

+3V

+3V\_ALW





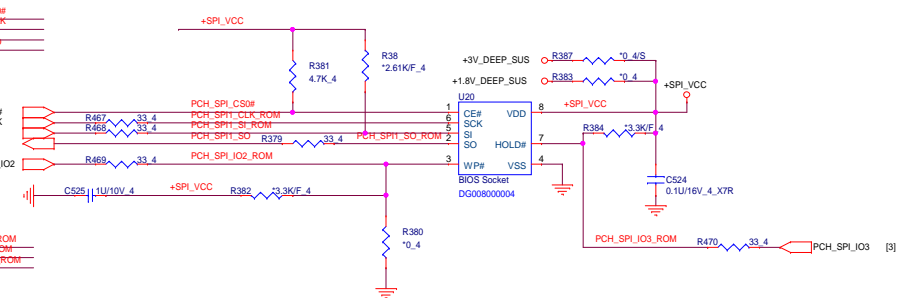
Vender	Size	P/N
Winbond	8MB	AKE3EFPKN01
Winbond	16MB	AKE3DZN0N01 SI :02' 02
Socket		DFHS08FS046

## PCH SPI ROM(CLG)

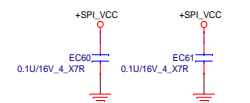
TP1047  
TP1048  
TP1049  
TP1050

[3,48] PCH\_SPI\_CS0#  
[3,34,48] PCH\_SPI1\_CLK  
[3,34,48] PCH\_SPI1\_SI  
[3,34,48] PCH\_SPI1\_SO

TP1051  
TP1052  
TP1053

PCH 6\*5mm WSON 16M  
SPI ROM Socket

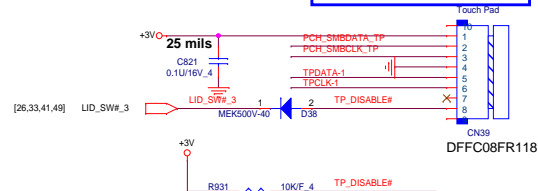
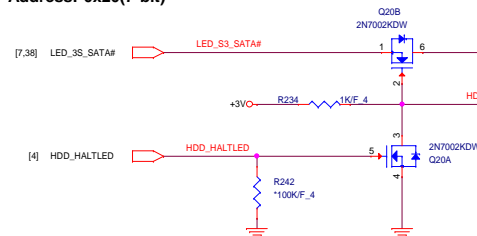
## For EMI Reserved



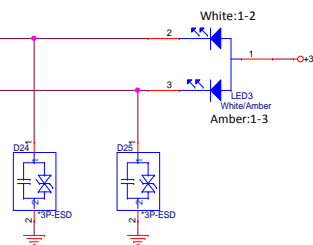
## Touch pad



## Forced Pad Connector

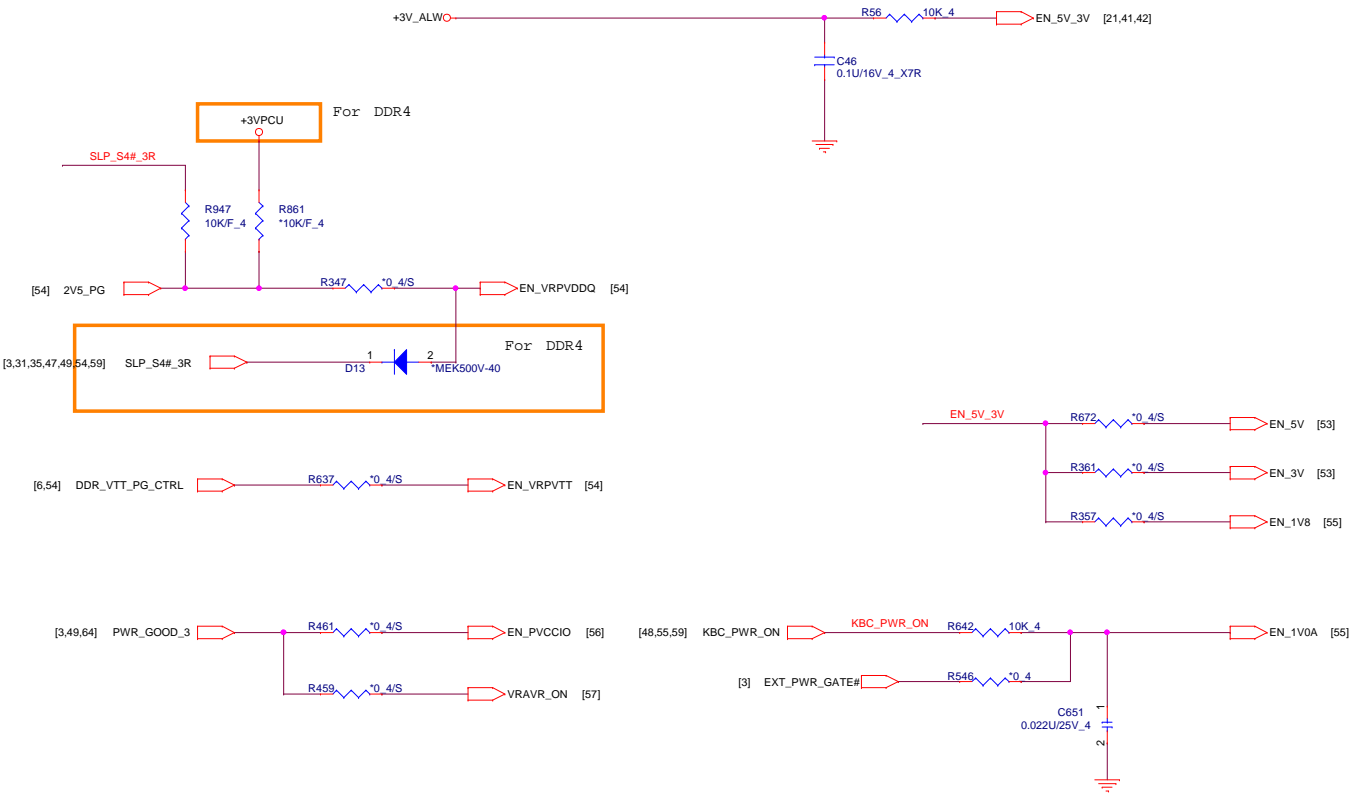
CLICK PAD  
Address: 0x20(7 bit)

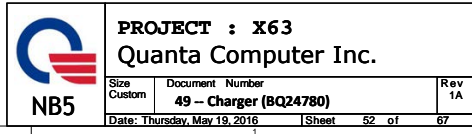
## HDD LED



PROJECT : X63  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	47 - Flash(KBC+PCH)/ Touch pad	1A
Date: Thursday, Mar 19, 2016	Sheet 50 of 67	

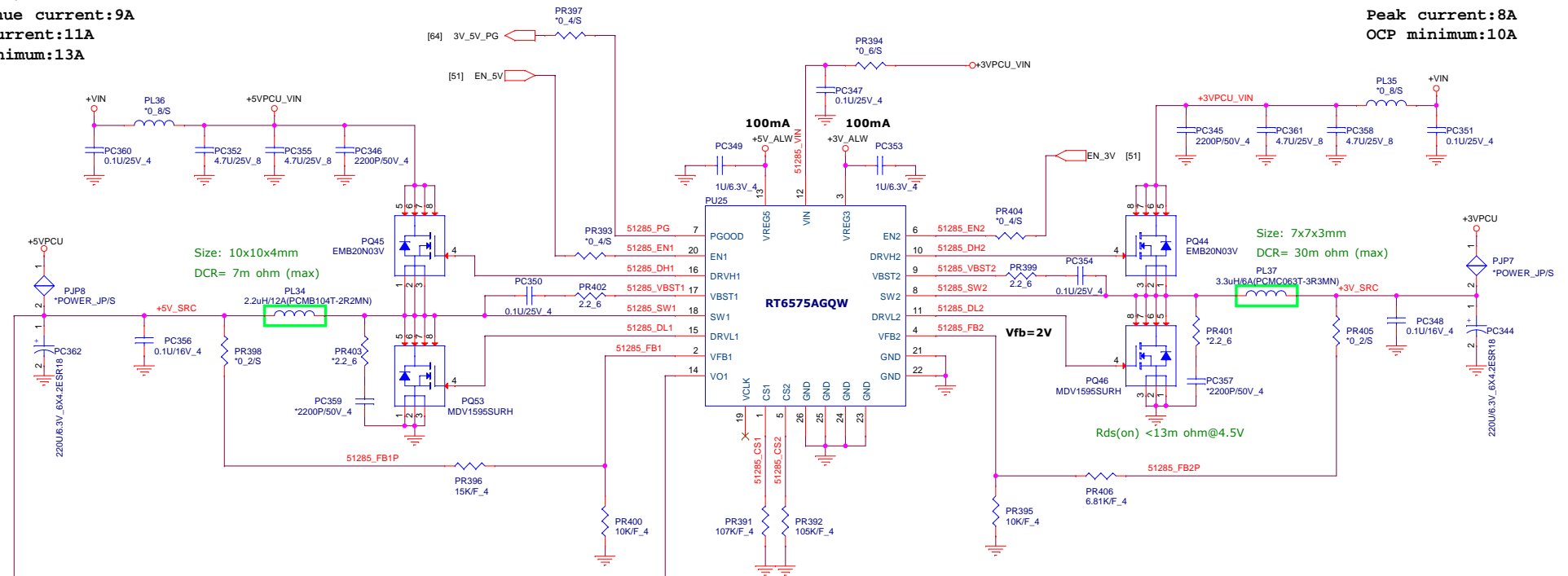


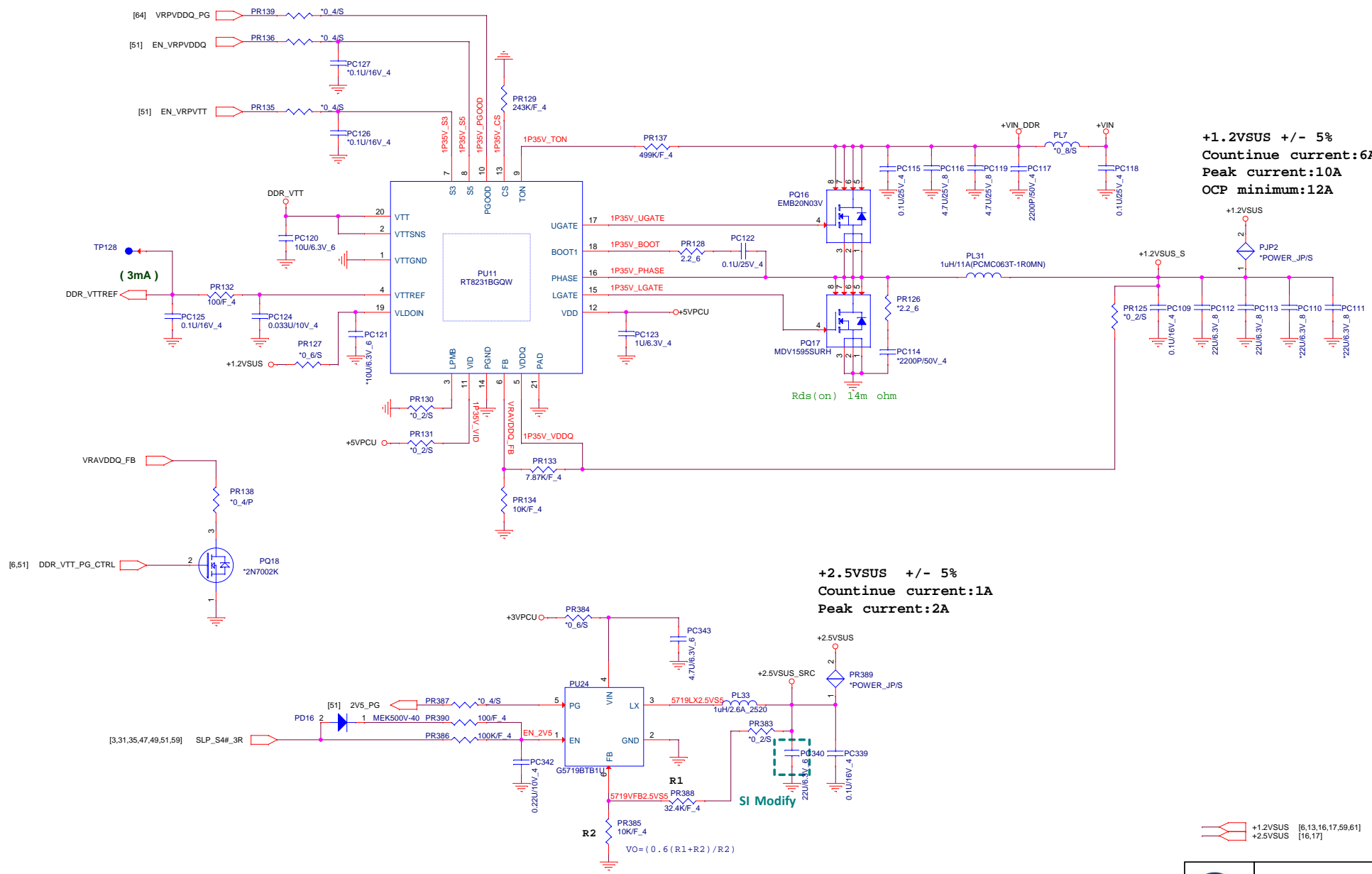


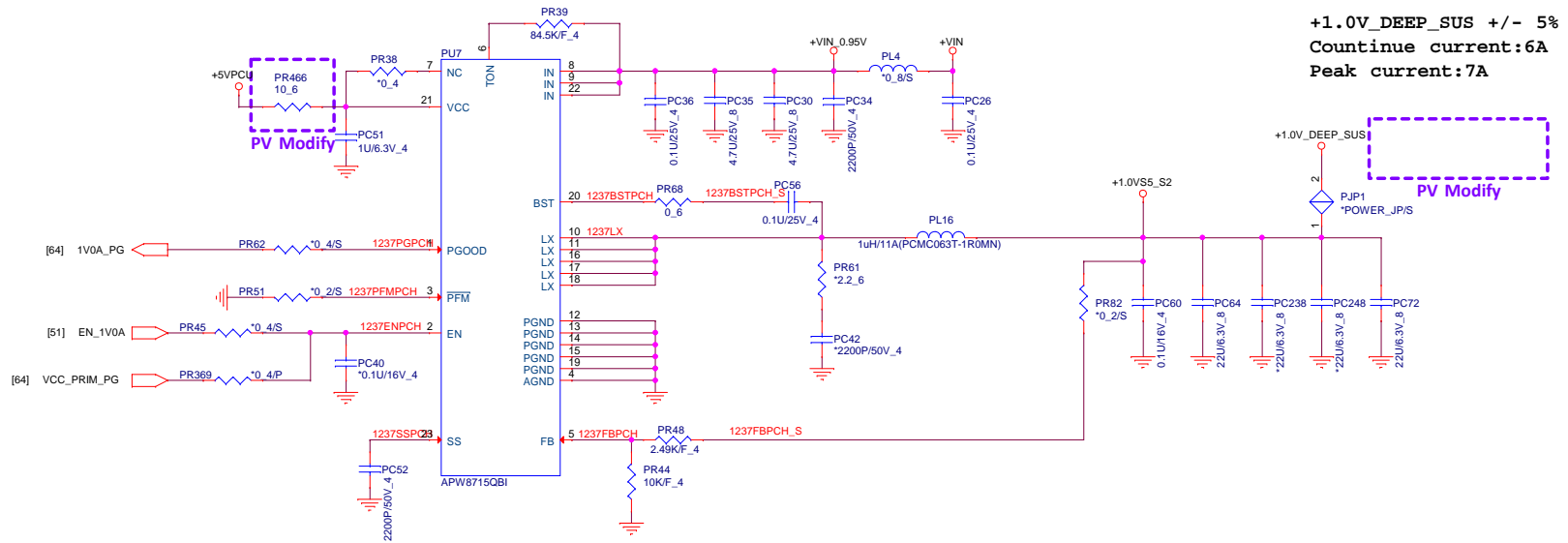
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,54,56,59,61,63,64,67]  
+5VPCU [31,35,44,45,46,47,52,54,55,57,58,59,60,61,62,64,67]

+5VPCU +/- 5%  
Countinue current:9A  
Peak current:11A  
OCP minimum:13A

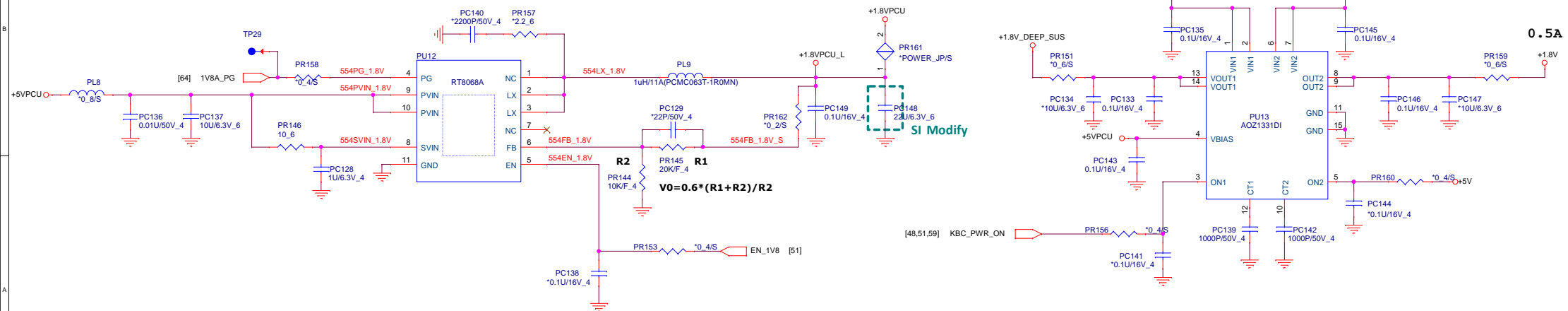
+3VPCU +/- 5%  
Countinue current:6A  
Peak current:8A  
OCP minimum:10A



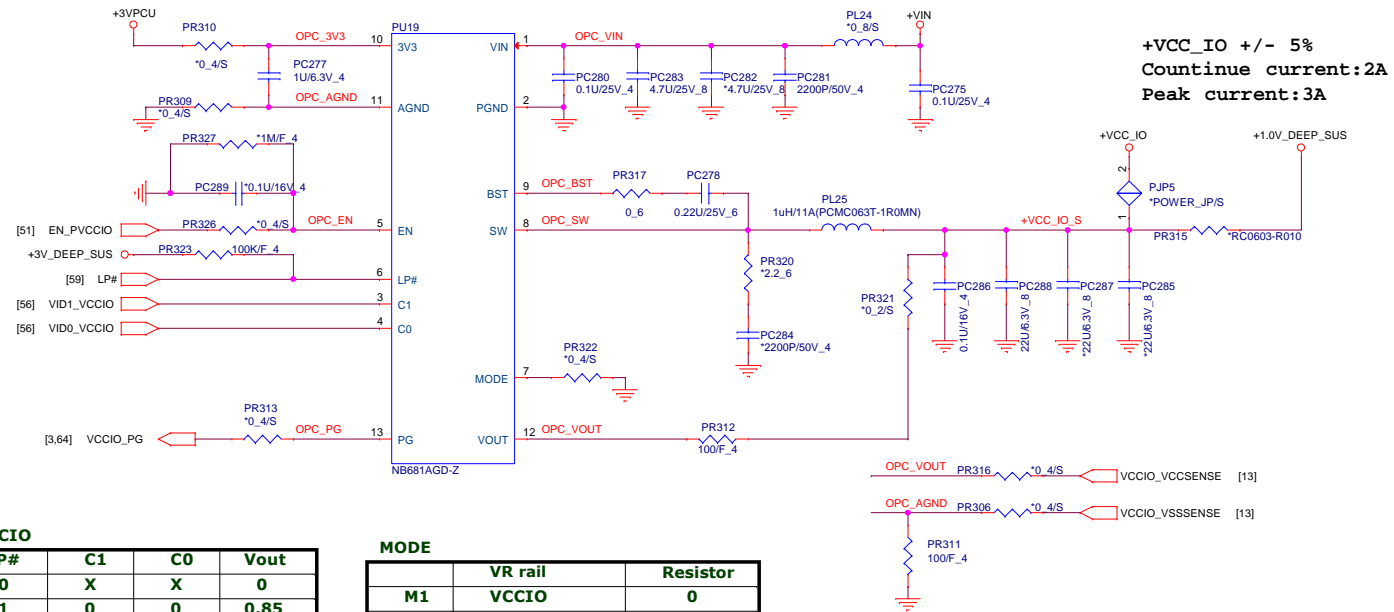




**+1.8VPCU +/- 5%**  
**Countinue current:2A**  
**Peak current:4A**



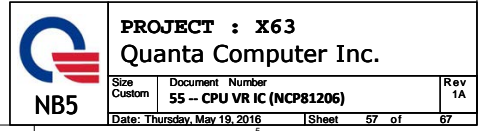
+VIN [26,43,47,52,53,54,56,57,58,59,60,62,67]  
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]  
+5VPCU [31,35,44,45,46,47,52,53,54,57,58,59,60,61,62,64,67]

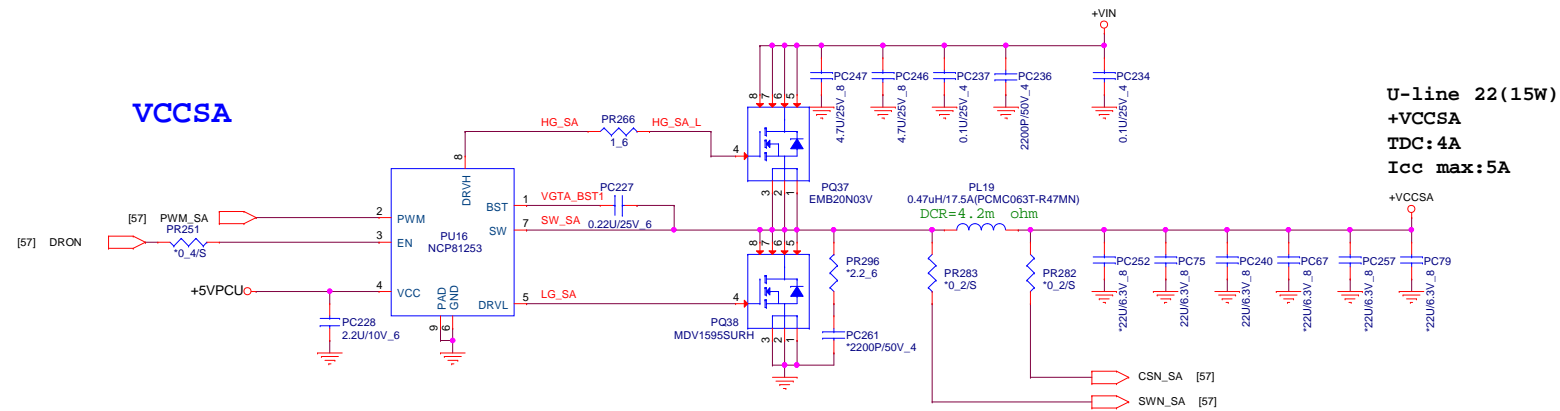


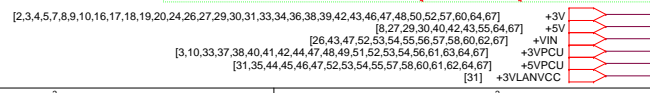
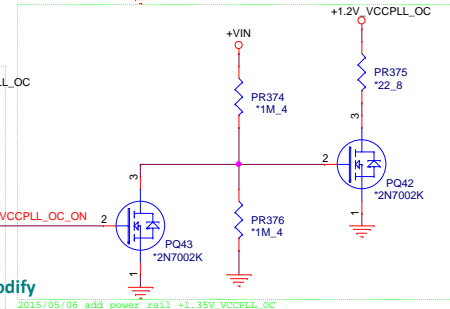
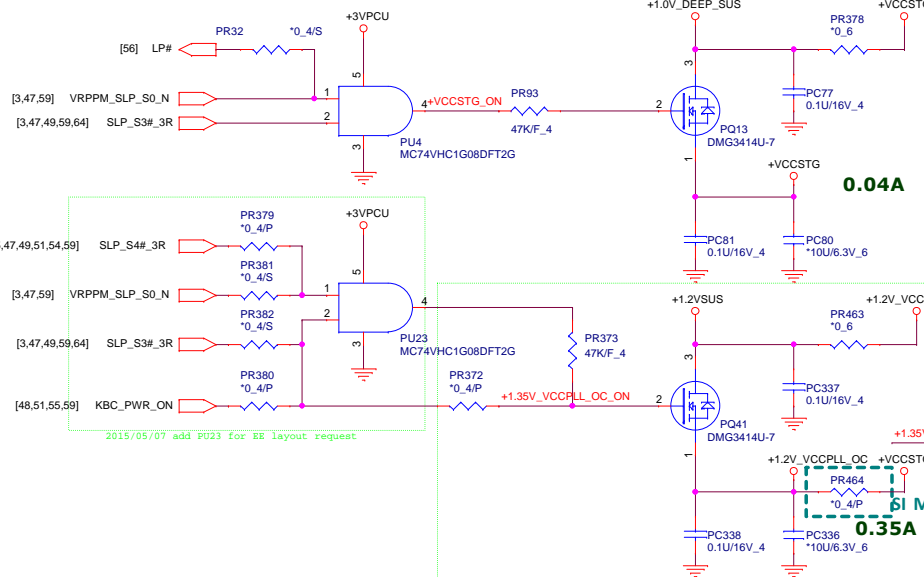
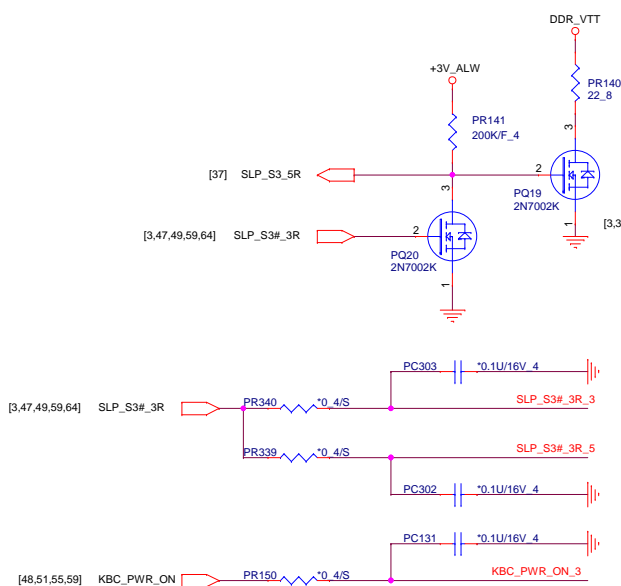
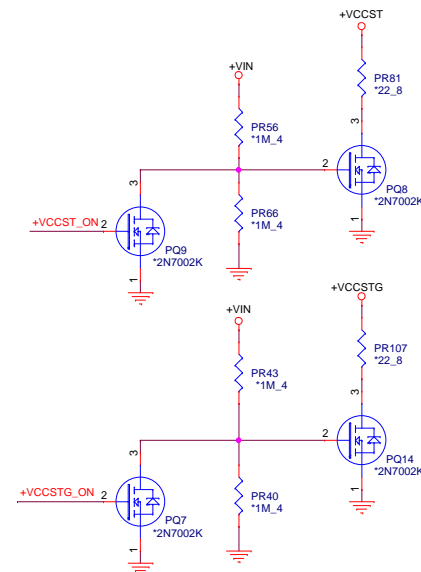
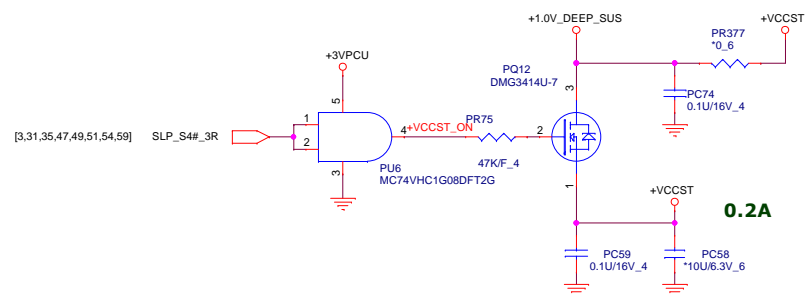
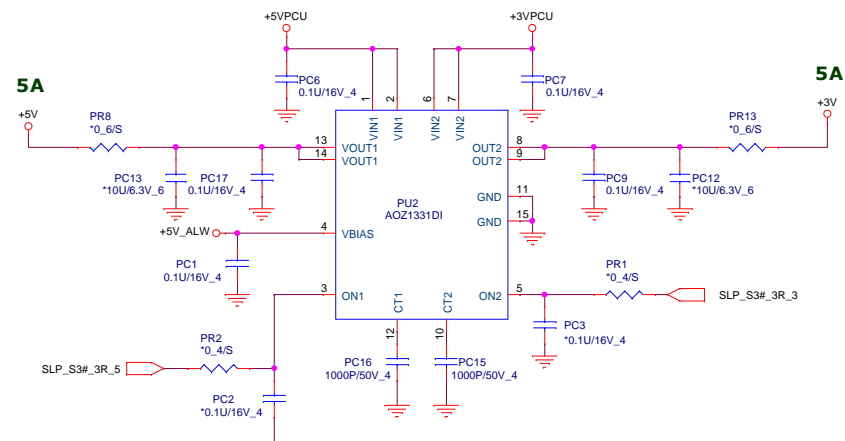
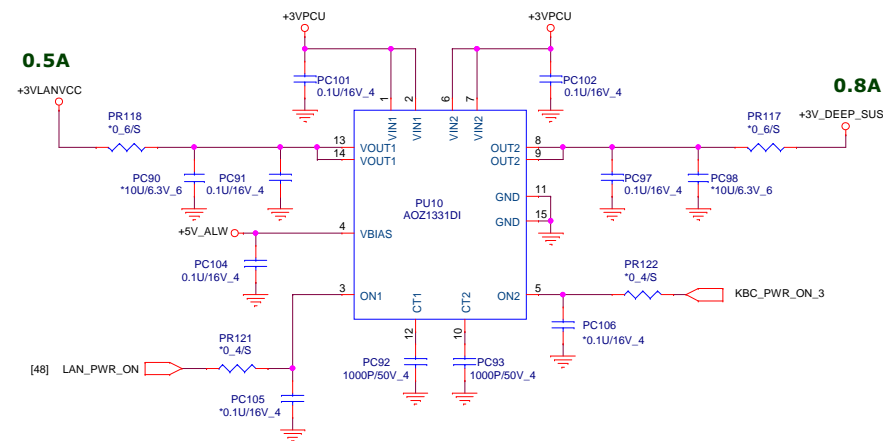
VCCIO			
LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE		
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K



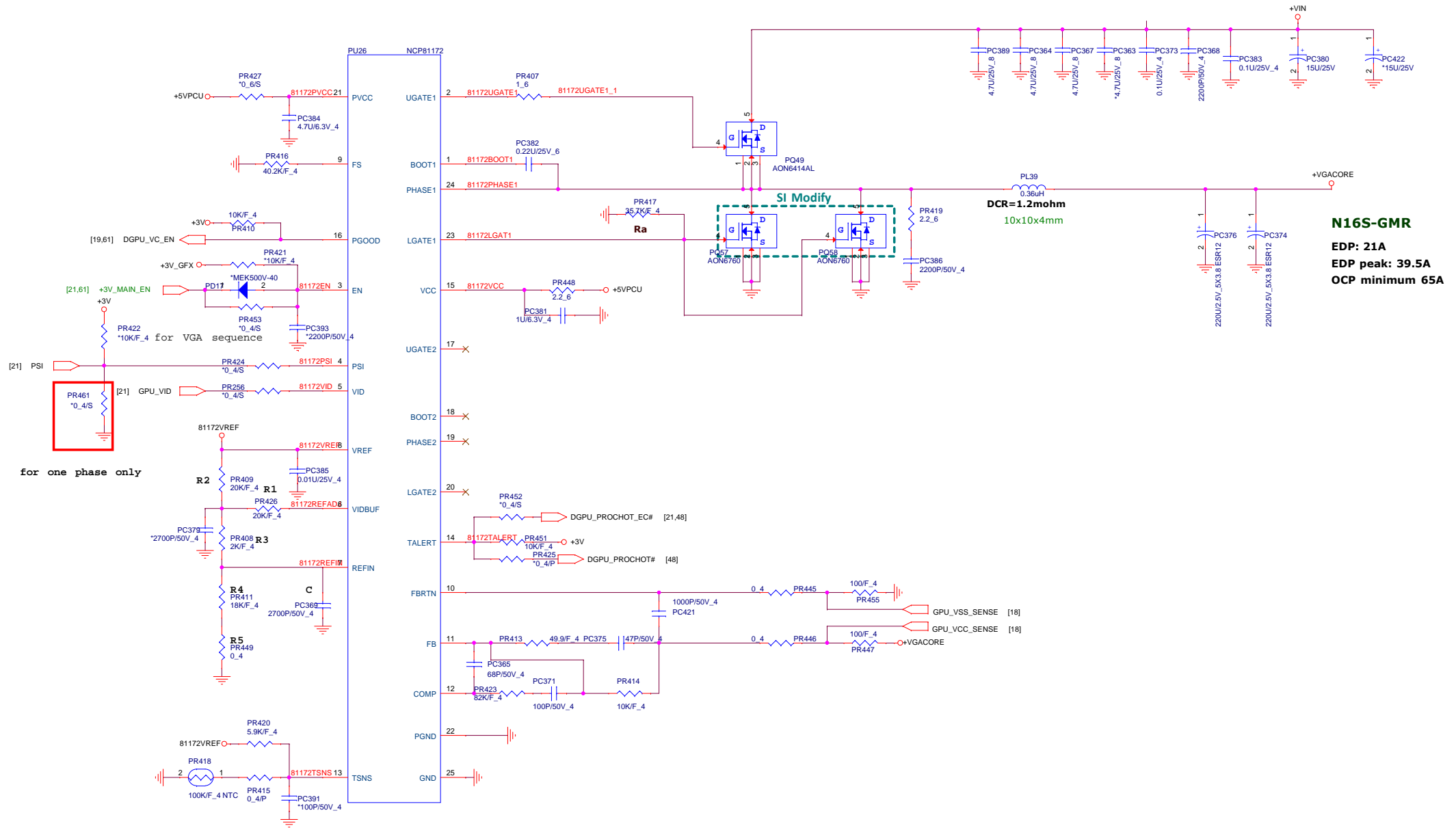


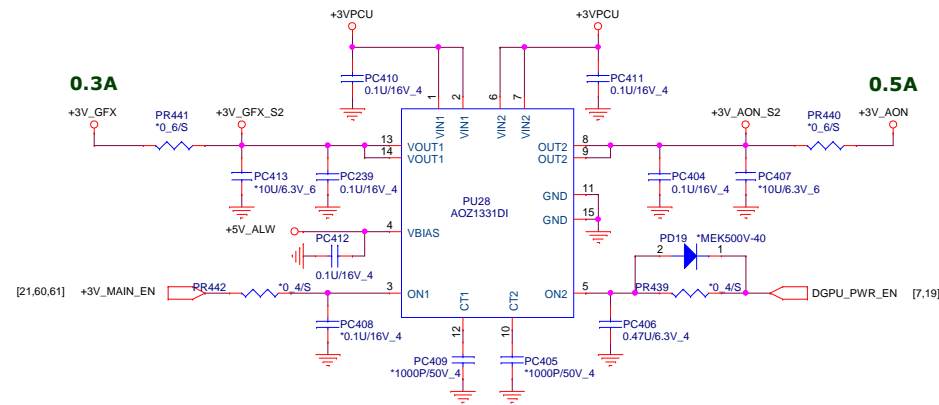
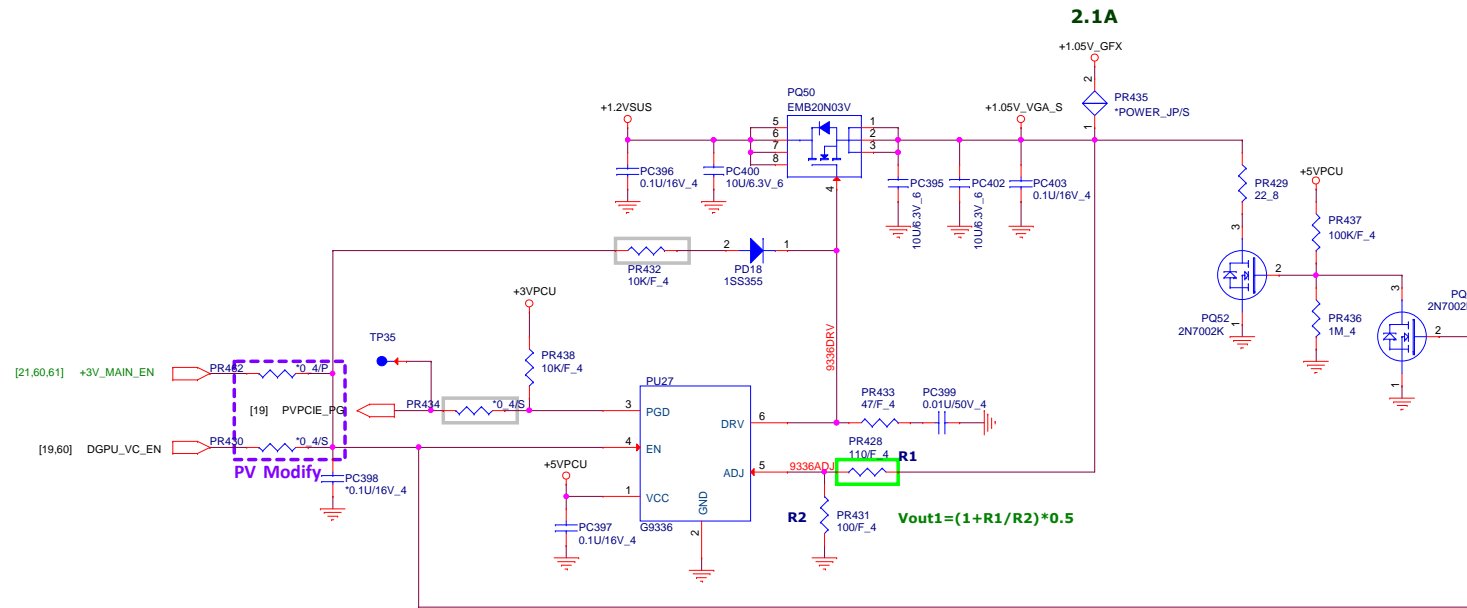




**PROJECT : X63**  
**Quanta Computer Inc.**

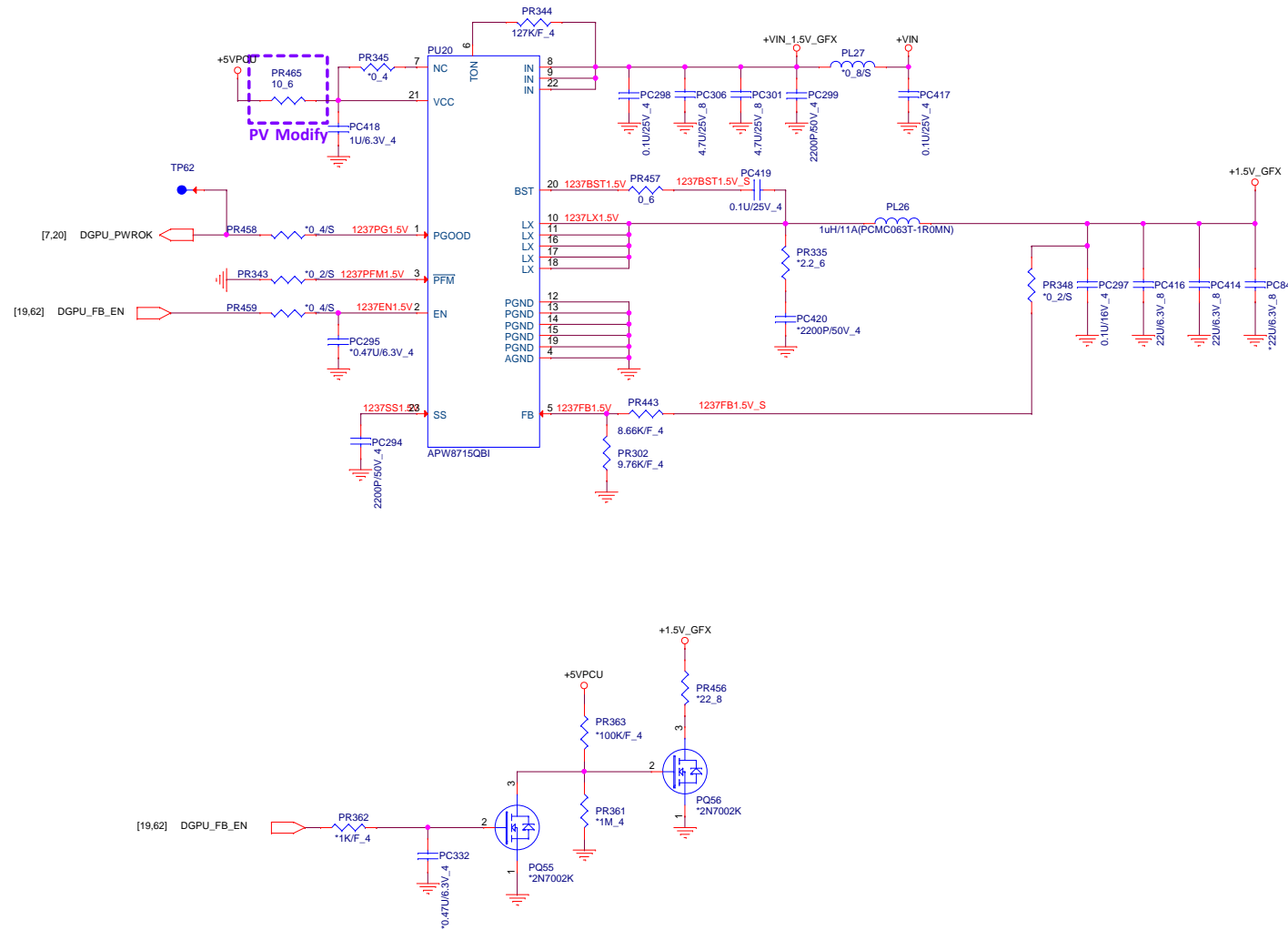
Size	Document Number	Rev
Custom	57 -- Load switch IC (APL3523A)	1A
Date: Thursday, May 19, 2016	Sheet 59 of 67	



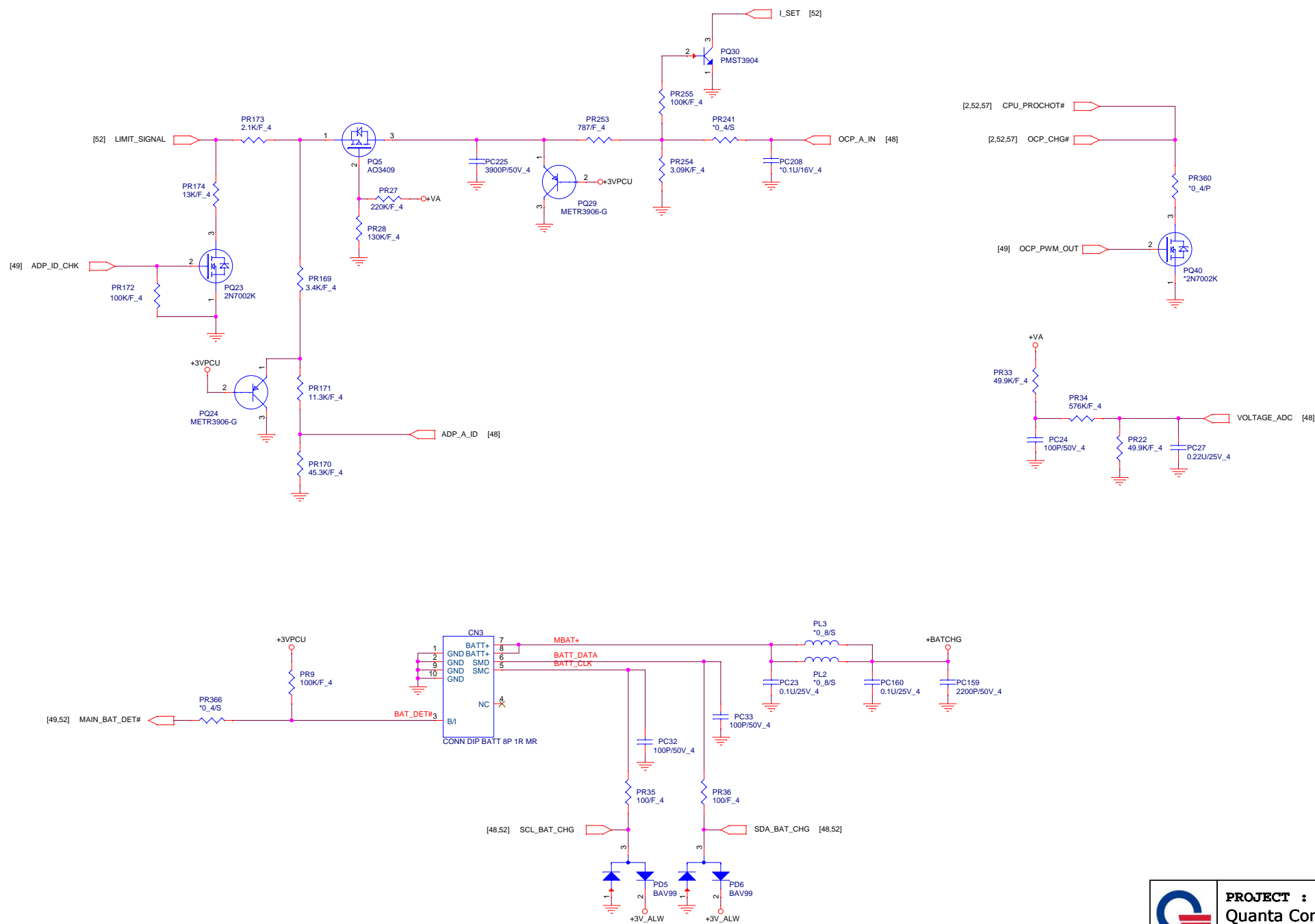


**PROJECT : X63**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	60 -- +1.0V_VGA/1.8V_VGA/3V_VGA	1A
Date: Thursday, May 19, 2016	Sheet 61 of 67	



# Adapter OCP



# POK CKT

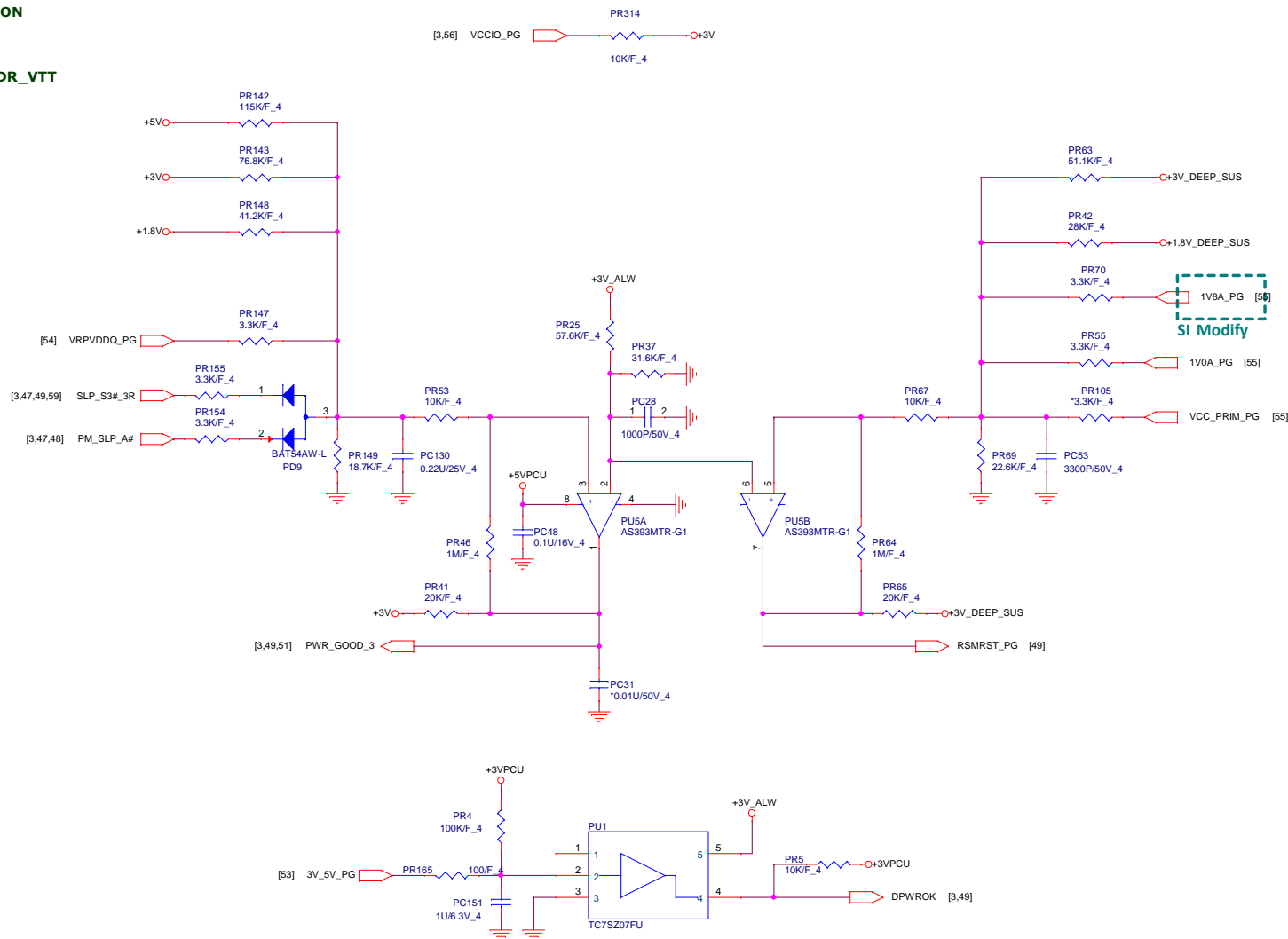
PM\_SLP\_S4# = SUSON

PM\_SLP\_S3# = MAINON

+V5S = +5V


+V3S = +3V

+V0.75S = +0.75V\_DDR\_VTT



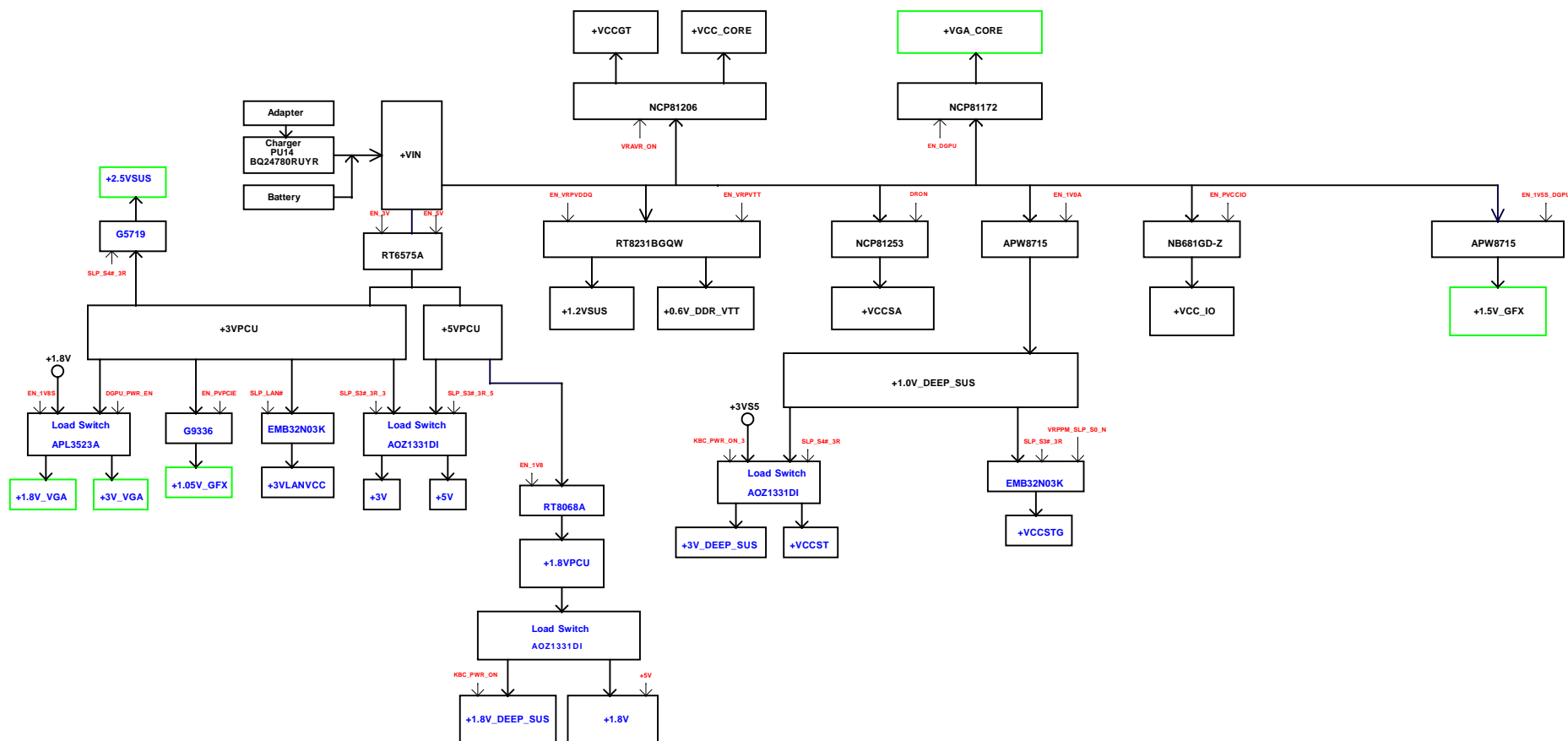
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,67]  
[6,27,29,30,40,42,43,55,59,67]  
[9,41,51,52,53,59,63,67]

+V5V  
+V3V  
+V0.75V

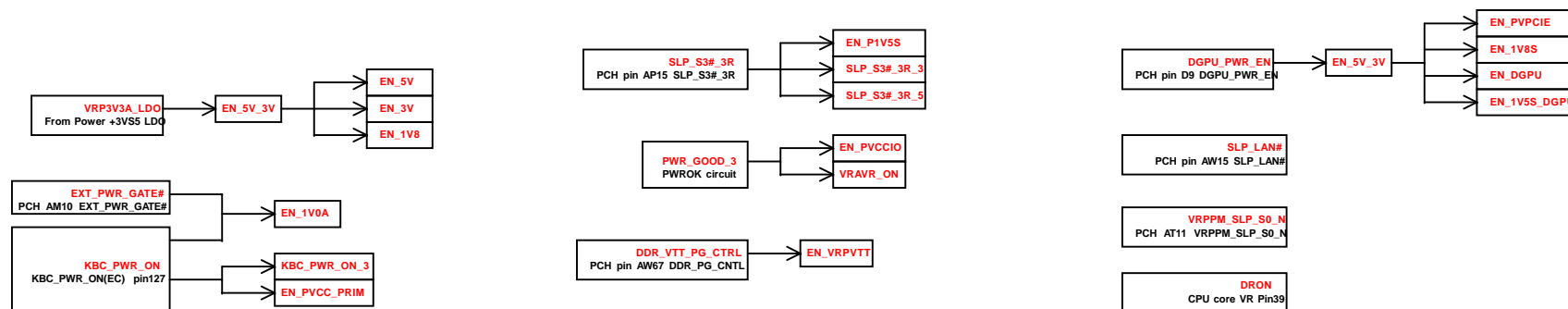
 NB5	<b>PROJECT : X63</b> <b>Quanta Computer Inc.</b>				Rev 1A
	Size Custom	Document Number <b>63 -- PWROK</b>			
	Date: Thursday, May 19, 2016		Sheet 64 of	67	



# POWER BLOCK DIAGRAM

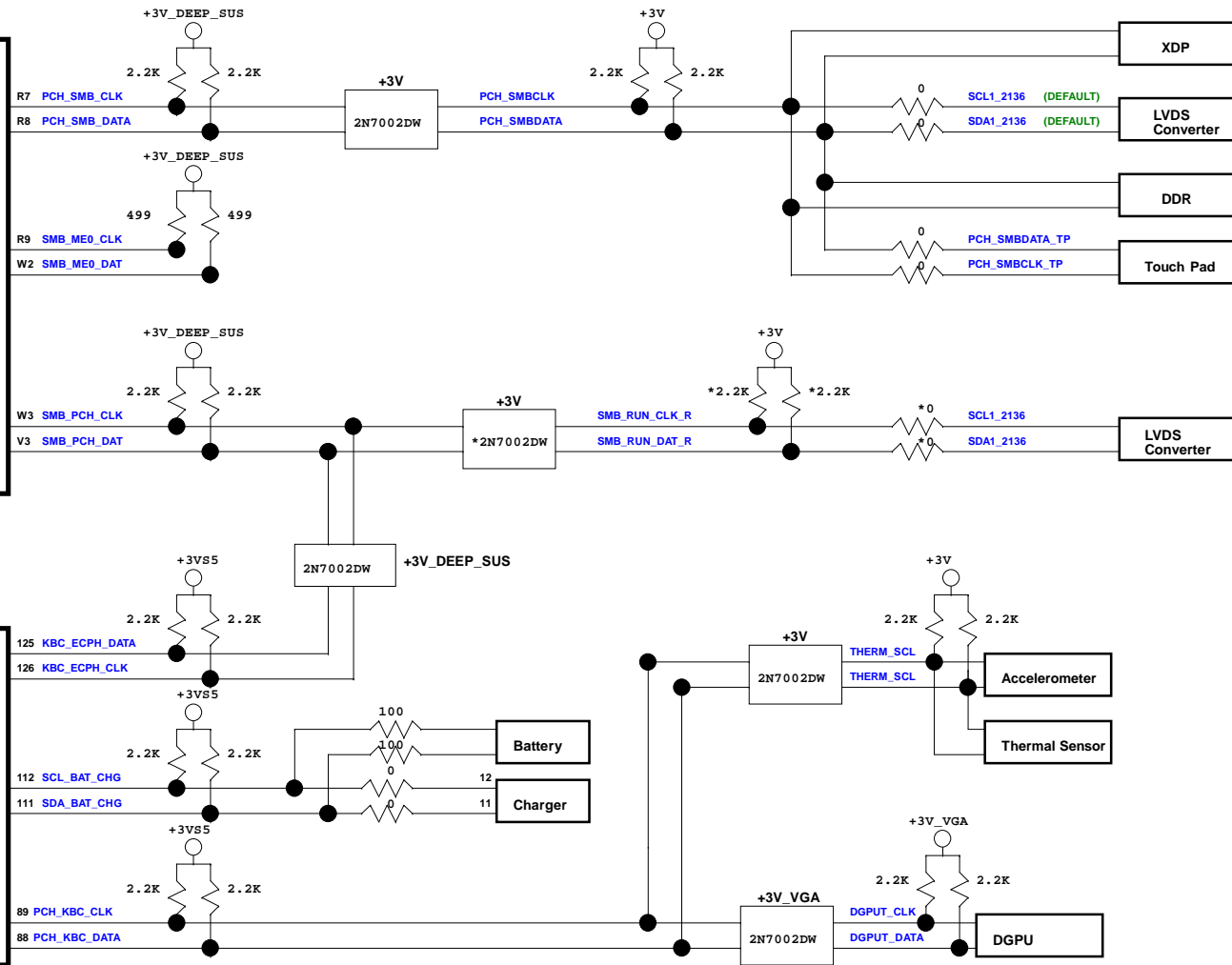


## POWER ENABLE PIN



SKYLAKE U

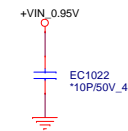
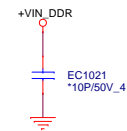
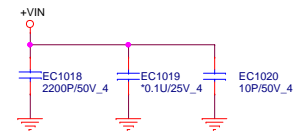
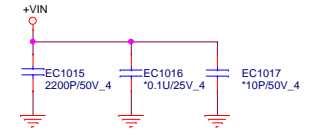
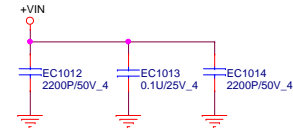
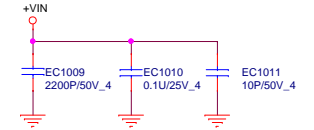
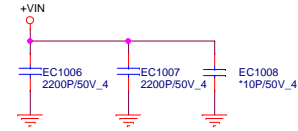
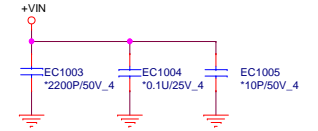
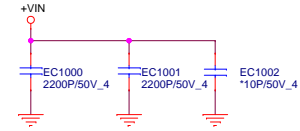
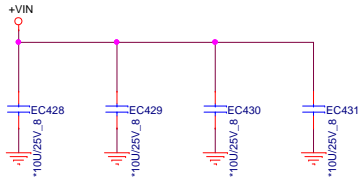
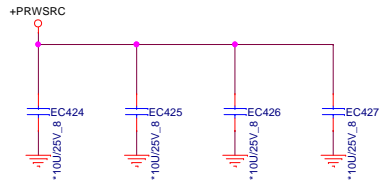
EC  
NPCE586H



Example: \*499/F\_4 and \*0\_6/S  
 \* means none-installed  
 499 means value  
 F means 1%  
 \_4 means 0402 size  
 /S means short pad

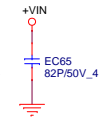
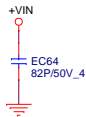
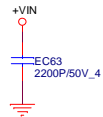
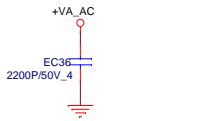
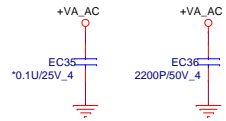
Mult i plexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Lef t s i de do wn)
USB2 #2	USB2.0/USB3.0 Combo Jack(Lef t s i de up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

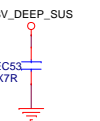
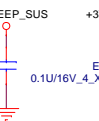
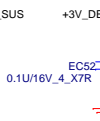
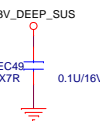
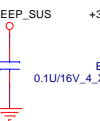
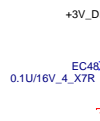
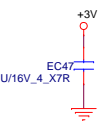
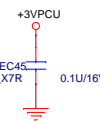
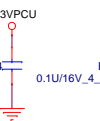
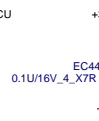
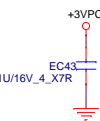
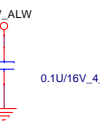
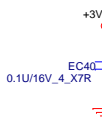
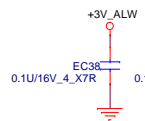


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